LAN8804

4-Port Gigabit Ethernet Transceiver with QSGMII Support

Features

- Quad-Port Gigabit Ethernet Transceiver
- QSGMII Version 1.3 MAC Interface
- Jumbo Frame Support Up to 16 KB
- Clocked from Crystal or External 25/125 MHz Reference Clock Input
- Time Sensitive Networking (TSN) Frame Preemption support per IEEE 802.3™-2018 clause 99
- IEEE 802.3-2018 Energy Efficient Ethernet (EEE)
- Two Programmable LED Outputs per Port for Link, Activity, and Speed
- Coma mode to Eliminate Port Link Bouncing at Startup and Synchronize LEDs
- 24 GPIOs
- LinkMD® TDR-based Cable Diagnostic to Identify Faulty Copper Cabling
- Signal Quality Indication
- Loopback modes for Diagnostics
- Automatic MDI/MDI-X Crossover to Detect and Correct Pair Swaps, Pair Skew, and Pair Polarity
- Shared Management Data Input/Output (MDIO) Interface for PHY Register Configuration
- Interrupt Pin Option
- Die Temperature Monitor
- Power-Down and Power-Saving Modes
  - Energy Detect Power Down
  - Chip Power Down
  - EEE Low Power Idle mode
  - Smart power savings up to 20 mW for cables <70m
- Operating Voltages
  - Digital Core (VDDCORE): 1.21V
  - Analog Operation: 1.21V (VDDAL) and 2.5V, 3.3V (VDD33REF)
  - VDD I/O (VDDIO): 3.3V, 2.5V, or 1.8V
  - Transceiver (VDDAH): 3.3V or 2.5V
- 128-pin TQFP (14 × 14 mm body) Package
- Temperature Support
  - Commercial temperature range (0° to +85°C)
  - Industrial temperature range (-40° to +85°C)

Target Applications

- Enterprise/SMB Switches
- Industrial Switches
- Cellular Infrastructure
- Routers
- Wi-Fi Access Points
- Gateways
- FPGA Based Systems
- General Embedded

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1.0 PREFACE

1.1 General Terms

TABLE 1-1: GENERAL TERMS

Term	Description
1000BASE-T	1 Gbps Ethernet over twisted pair, IEEE 802.3 compliant
100BASE-TX	100 Mbps Ethernet over twisted pair, IEEE 802.3 compliant
10BASE-T	10 Mbps Ethernet over twisted pair, IEEE 802.3 compliant
10BASE-Te	Energy-efficient version of 10BASE-T, IEEE 802.3 compliant
ADC	Analog-to-Digital Converter
AFE	Analog Front End
AGC	Automatic Gain Control
AN	Auto-Negotiation
AWG	Additive White Gaussian
BER	Bit Error Rate
Byte	8 bits
DCQ	Dynamic Channel Quality
DSP	Digital Signal Processing
EDPD	Energy-Detect Power-Down
EEE	Energy Efficient Ethernet
EMI	Electromagnetic interference
FCS	Frame Check Sequence
FIFO	First In First Out buffer
FLP	Fast Link Pulse
GMII	Gigabit Media Independent Interface
GPIO	General Purpose I/O
HBM	Human Body Model. Simulates ESD from humans.
ISI	Inter-symbol interference
JTP	Jitter Test Pattern
LDO	Linear Drop-Out regulator
LFSR	Linear Feedback Shift Register
LPI	Low Power Idle
MAC	Media Access Controller

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TABLE 1-1: GENERAL TERMS (CONTINUED)

Term	Description
MDI	Medium Dependent Interface
MDIO	Management Data Input/Output
MDIX	Media Dependent Interface with crossover
MII	Media Independent Interface
MLT-3	Multi-Level Transmission Encoding (3-levels). A tri-level encoding method where a change in the logic level represents a code bit “1” and the logic output remaining at the same level represents a code bit “0”
N/A	Not Applicable
NC	No Connect
NLP	Normal Link Pulse
MMD	MDIO Manageable Device
MSE	Mean Squared Error
PAM5	5-level Pulse Amplitude Modulation
PCS	Physical Coding Sublayer
PEC	Packet-based Equipment Clock
PHY	Physical layer
PLL	Phase-Locked Loop
POR	Power On Ready
PTP	Precision Time Protocol
QSGMII	Quad Serial Gigabit Media Independent Interface
RESERVED	Refers to a reserved bit field or address. Unless otherwise noted, reserved bits must always be zero for write operations. Unless otherwise noted, values are not guaranteed when reading reserved bits. Unless otherwise noted, do not read or write to reserved addresses.
SerDes	Serializer/Deserializer
SFD	Start of Frame Delimiter. The 8-bit value indicating the end of the preamble of an Ethernet frame.
SMD	Start mPacket Delimiter
SNR	Signal to Noise Ratio
SoC	System-on-Chip
SOF	Start of Frame
SPD	Start of Packet Delimiter. Used in QSGMII
	Software Power-Down

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TABLE 1-1: GENERAL TERMS (CONTINUED)

Term	Description
SQI	Signal Quality Index
STI	Serial Timestamp Interface
TDR	Time Domain Reflectometry
TQFP	Thin Quad Flat Pack
TSN	Time Sensitive Networking
TSU	Time Stamp Unit
UDP	User Datagram Protocol. A connectionless protocol run on top of IP networks.
UTP	Unshielded Twisted Pair

1.2 Buffer Types

TABLE 1-2: BUFFER TYPE DESCRIPTIONS

Buffer	Description
AI	Analog input
AO	Analog output
AIO	Analog bidirectional
GND	Ground pin
ICLK	Crystal oscillator input pin
LVDS1	LVDS1 input pin
LVDS2	LVDS2 input pin
OCLK	Crystal oscillator output pin
SRL	Slew Rate Limited output
VIS	Variable voltage Schmitt-triggered input
VO12	Variable voltage output with 12 mA sink and 12 mA source
VOD12	Variable voltage open-drain output with 12 mA sink
VOS12	Variable voltage open-source output with 12 mA source
PU	70 kΩ (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are always enabled. **Note:** Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
PD	70 kΩ (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are always enabled. **Note:** Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
P	Power pin

Note: Digital signals are not 5V tolerant unless specified.

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1.3 Pin Reset States

The pin reset state definitions are detailed in Table 1-3. Refer to Table 3-1 for details on individual pin reset states.

TABLE 1-3: PIN RESET STATE LEGEND

Symbol	Description
AI	Analog input
AO	Analog output
PD	Hardware enables pull-down
PU	Hardware enables pull-up
Y	Hardware enables function
Z	Hardware disables output driver (high impedance)

1.4 Reference Documents

1. *IEEE Standard for Ethernet*, IEEE 802.3-2018, https://standards.ieee.org/standard/802_3-2018.html
2. *IEEE Standard for Ethernet Amendment 5: Specification and Management Parameters for Interspersing Express Traffic*, IEEE 802.3br™-2016, https://standards.ieee.org/standard/802_3br-2016.html
3. *IEEE Standard for Local and Metropolitan Area Networks Bridges and Bridged Networks Amendment 26: Frame Preemption*, IEEE 802.1Qbu™-2016, https://standards.ieee.org/standard/802_1Qbu-2016.html
4. *Cisco QSGMII Specification*, EDCS-540123 Rev. 1.3

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2.0 INTRODUCTION

2.1 General Description

The LAN8804 is a low-power, quad-port triple-speed (10BASE-T/100BASE-TX/1000BASE-T) Ethernet physical layer transceiver (PHY) that supports transmission and reception of data on standard CAT-5, as well as CAT-5e and CAT-6, Unshielded Twisted Pair (UTP) cables.

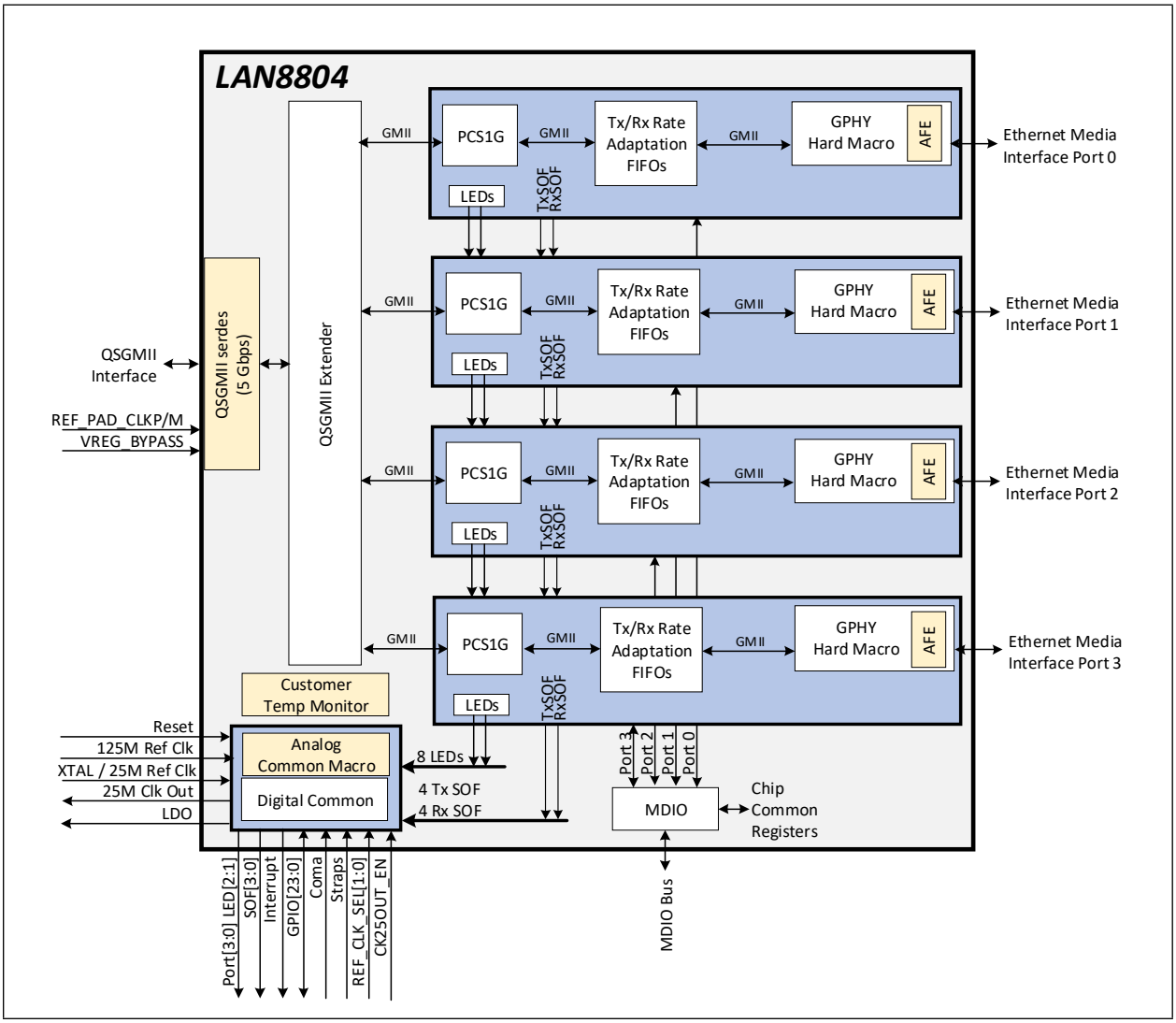
The LAN8804 supports industry-standard QSGMII (Quad Serial Gigabit Media Independent Interface) providing chip-to-chip connection to four Gigabit Ethernet MACs using a single serialized link (differential pair) in each direction.

The LAN8804 reduces board cost and simplifies board layout by using on-chip termination resistors for the line-facing differential pairs.

The LAN8804 offers diagnostic features to facilitate system bring-up and debugging in production testing and in product deployment. The LinkMD TDR-based cable diagnostic identifies faulty copper cabling. Integrated loopback functions verify analog and digital data paths.

The LAN8804 is available in a 128-pin, RoHS Compliant TQFP package with commercial (0°C to +85°C) and industrial (-40°C to +85°C) temperature ranges. An internal block diagram of the LAN8804 is shown in Figure 2-1.

FIGURE 2-1: INTERNAL BLOCK DIAGRAM



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The LAN8804 is designed for two primary target applications:

- Switch Application
- SoC Application

Figure 2-2 details a 64 Gbps industrial Ethernet switch configuration example that is based on the Microchip VSC7546 SparX-5i and six LAN8804 PHYs. The 24x 1 GbE + 4x 10 GbE is a typical configuration for the 64 Gbps Stock Keeping Unit. The SparX-5i industrial Ethernet switch family is available in 64 Gbps through 200 Gbps and supports up to 48x 1 GbE using twelve QSGMII interfaces.

FIGURE 2-2: SWITCH APPLICATION

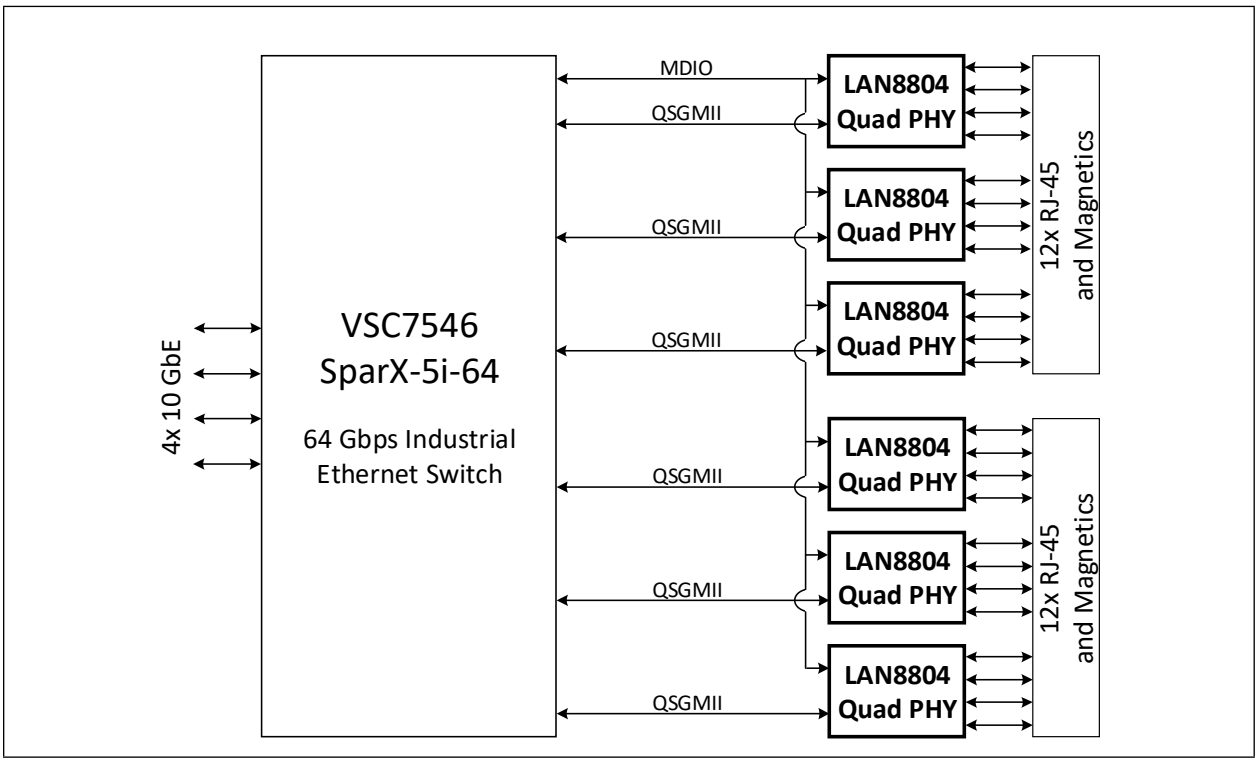
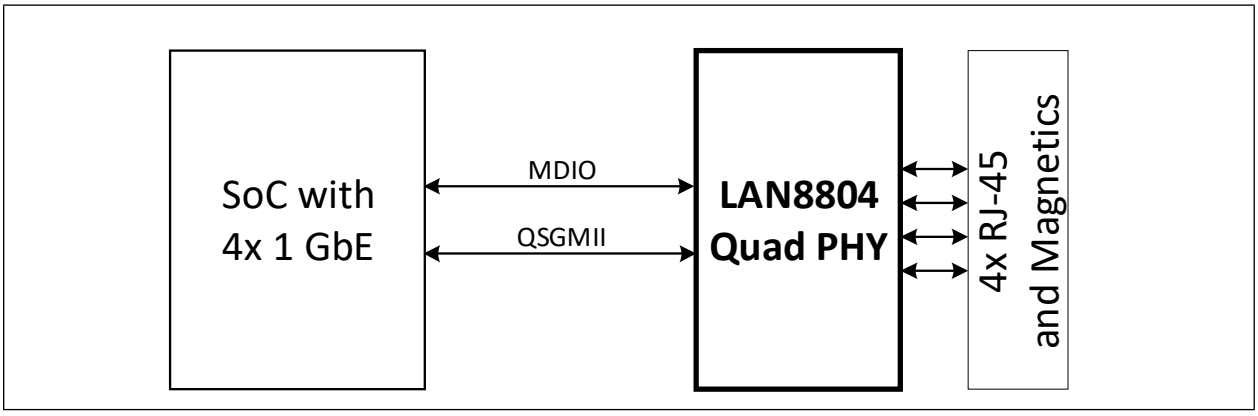


Figure 2-3 details a typical 4 Gbps industrial Ethernet System-on-Chip (SoC) application using a single LAN8804 PHY.

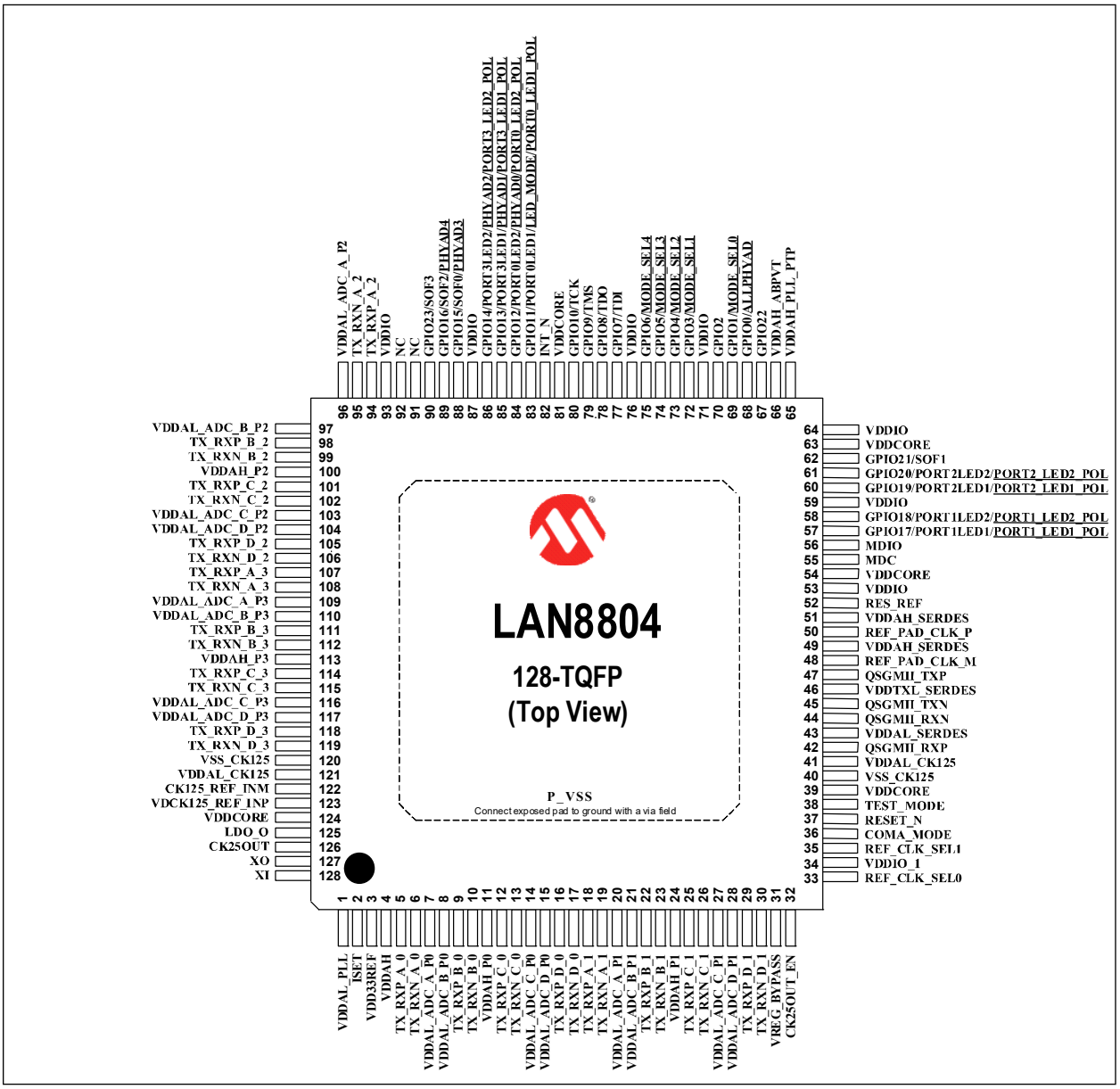
FIGURE 2-3: SOC APPLICATION



3.0 PIN DESCRIPTIONS AND CONFIGURATION

3.1 Pin Assignments

FIGURE 3-1: PIN ASSIGNMENTS (TOP VIEW)



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TABLE 3-1: PIN ASSIGNMENTS

Pin Num.	Pin Name	Reset	Pin Num.	Pin Name	Reset
1	VDDAL_PLL	Z	65	VDDAH_PLL_PTP	Z
2	ISET	AI	66	VDDAH_ABPVT	Z
3	VDD33REF	Z	67	GPIO22	PD
4	VDDAH	Z	68	GPIO0/ALLPHYAD	PD
5	TX_RXP_A_0	AI	69	GPIO1/MODE_SEL0	PD
6	TX_RXN_A_0	AI	70	GPIO2	Z
7	VDDAL_ADC_A_P0	Z	71	VDDIO	Z
8	VDDAL_ADC_B_P0	Z	72	GPIO3/MODE_SEL1	PD
9	TX_RXP_B_0	AI	73	GPIO4/MODE_SEL2	PD
10	TX_RXN_B_0	AI	74	GPIO5/MODE_SEL3	PU
11	VDDAH_P0	Z	75	GPIO6/MODE_SEL4	PU
12	TX_RXP_C_0	AI	76	VDDIO	AI
13	TX_RXN_C_0	AI	77	GPIO7/TDI	Z
14	VDDAL_ADC_C_P0	Z	78	GPIO8/TDO	Z
15	VDDAL_ADC_D_P0	Z	79	GPIO9/TMS	Z
16	TX_RXP_D_0	AI	80	GPIO10/TCK	Z
17	TX_RXN_D_0	AI	81	VDDCORE	AI
18	TX_RXP_A_1	AI	82	INT_N	PU
19	TX_RXN_A_1	AI	83	GPIO11/PORT0LED1/LED_MODE/ PORT0_LED1_POL	PD
20	VDDAL_ADC_A_P1	Z	84	GPIO12/PORT0LED2/PHYAD0/ PORT0_LED2_POL	PD
21	VDDAL_ADC_B_P1	Z	85	GPIO13/PORT3LED1/PHYAD1/ PORT3_LED1_POL	PD
22	TX_RXP_B_1	AI	86	GPIO14/PORT3LED2/PHYAD2/ PORT3_LED2_POL	PD
23	TX_RXN_B_1	AI	87	VDDIO	Z
24	VDDAH_P1	Z	88	GPIO15/SOF0/PHYAD3	PD
25	TX_RXP_C_1	AI	89	GPIO16/SOF2/PHYAD4	PD
26	TX_RXN_C_1	AI	90	GPIO23/SOF3	PD
27	VDDAL_ADC_C_P1	Z	91	NC	PD
28	VDDAL_ADC_D_P1	Z	92	NC	PD
29	TX_RXP_D_1	AI	93	VDDIO	Z
30	TX_RXN_D_1	AI	94	TX_RXP_A_2	AI
31	VREG_BYPASS	PU	95	TX_RXN_A_2	AI
32	CK25OUT_EN	PD	96	VDDAL_ADC_A_P2	Z
33	REF_CLK_SEL0	PU	97	VDDAL_ADC_B_P2	Z
34	VDDIO_1	Z	98	TX_RXP_B_2	AI
35	REF_CLK_SEL1	PU	99	TX_RXN_B_2	AI
36	COMA_MODE	PD	100	VDDAH_P2	Z
37	RESET_N	PU	101	TX_RXP_C_2	AI
38	TEST_MODE	PD	102	TX_RXN_C_2	AI
39	VDDCORE	Z	103	VDDAL_ADC_C_P2	Z
40	VSS_CK125	Z	104	VDDAL_ADC_D_P2	Z
41	VDDAL_CK125	Z	105	TX_RXP_D_2	AI
42	QSGMII_RXP	AI	106	TX_RXN_D_2	AI
43	VDDAL_SERDES	AI	107	TX_RXP_A_3	AI
44	QSGMII_RXN	AI	108	TX_RXN_A_3	AI

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Pin Num.	Pin Name	Reset	Pin Num.	Pin Name	Reset
45	QSGMII_TXN	AO	109	VDDAL_ADC_A_P3	Z
46	VDDTXL_SERDES	Z	110	VDDAL_ADC_B_P3	Z
47	QSGMII_TXP	AO	111	TX_RXP_B_3	AI
48	REF_PAD_CLK_M	AI	112	TX_RXN_B_3	AI
49	VDDAH_SERDES	Z	113	VDDAH_P3	Z
50	REF_PAD_CLK_P	AI	114	TX_RXP_C_3	AI
51	VDDAH_SERDES	Z	115	TX_RXN_C_3	AI
52	RES_REF	AI	116	VDDAL_ADC_C_P3	Z
53	VDDIO	Z	117	VDDAL_ADC_D_P3	Z
54	VDDCORE	Z	118	TX_RXP_D_3	AI
55	MDC	Z	119	TX_RXN_D_3	AI
56	MDIO	Z	120	VSS_CK125	Z
57	GPIO17/PORT1LED1/PORT1_LED1_POL	PD	121	VDDAL_CK125	Z
58	GPIO18/PORT1LED2/PORT1_LED2_POL	PD	122	CK125_REF_INM	AI
59	VDDIO	Z	123	CK125_REF_INP	AI
60	GPIO19/PORT2LED1/PORT2_LED1_POL	PD	124	VDDCORE	AI
61	GPIO20/PORT2LED2/PORT2_LED2_POL	PD	125	LDO_O	AO
62	GPIO21/SOF1	PD	126	CK25OUT	AO
63	VDDCORE	Z	127	XO	AO
64	VDDIO	Z	128	XI	AI‘
Exposed Pad (P_VSS) must be connected to ground.					

The pin reset state definitions are detailed in Section 1.3, "Pin Reset States".

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3.2 Pin Descriptions

This section contains descriptions of the various LAN8804 pins. The "_N" symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. For example, **RESET_N** indicates that the reset signal is active low. When "_N" is not present after the signal name, the signal is asserted when at the high voltage level. The pin buffer type definitions are detailed in Section 1.2, "Buffer Types".

The pin function descriptions have been broken into functional groups as follows:

- Ethernet Media Interface Pins
- QSGMII Interface Pins
- System Clock Pins
- Miscellaneous Pins
- JTAG Pins
- Configuration Strap Input Pins
- Power and Ground Pins

TABLE 3-2: ETHERNET MEDIA INTERFACE PINS

Name	Symbol	Buffer Type	Description
Ethernet Port 0 TX/RX Positive Channel A	**TX_RXP_A_0**	AIO	Port 0 Channel A positive signal of differential pair
Ethernet Port 0 TX/RX Negative Channel A	**TX_RXN_A_0**	AIO	Port 0 Channel A negative signal of differential pair
Ethernet Port 0 TX/RX Positive Channel B	**TX_RXP_B_0**	AIO	Port 0 Channel B positive signal of differential pair
Ethernet Port 0 TX/RX Negative Channel B	**TX_RXN_B_0**	AIO	Port 0 Channel B negative signal of differential pair
Ethernet Port 0 TX/RX Positive Channel C	**TX_RXP_C_0**	AIO	Port 0 Channel C positive signal of differential pair
Ethernet Port 0 TX/RX Negative Channel C	**TX_RXN_C_0**	AIO	Port 0 Channel C negative signal of differential pair
Ethernet Port 0 TX/RX Positive Channel D	**TX_RXP_D_0**	AIO	Port 0 Channel D positive signal of differential pair
Ethernet Port 0 TX/RX Negative Channel D	**TX_RXN_D_0**	AIO	Port 0 Channel D negative signal of differential pair
Ethernet Port 1 TX/RX Positive Channel A	**TX_RXP_A_1**	AIO	Port 1 Channel A positive signal of differential pair
Ethernet Port 1 TX/RX Negative Channel A	**TX_RXN_A_1**	AIO	Port 1 Channel A negative signal of differential pair
Ethernet Port 1 TX/RX Positive Channel B	**TX_RXP_B_1**	AIO	Port 1 Channel B positive signal of differential pair
Ethernet Port 1 TX/RX Negative Channel B	**TX_RXN_B_1**	AIO	Port 1 Channel B negative signal of differential pair

TABLE 3-2: ETHERNET MEDIA INTERFACE PINS (CONTINUED)

Name	Symbol	Buffer Type	Description
Ethernet Port 1 TX/RX Positive Channel C	**TX_RXP_C_1**	AIO	Port 1 Channel C positive signal of differential pair
Ethernet Port 1 TX/RX Negative Channel C	**TX_RXN_C_1**	AIO	Port 1 Channel C negative signal of differential pair
Ethernet Port 1 TX/RX Positive Channel D	**TX_RXP_D_1**	AIO	Port 1 Channel D positive signal of differential pair
Ethernet Port 1 TX/RX Negative Channel D	**TX_RXN_D_1**	AIO	Port 1 Channel D negative signal of differential pair
Ethernet Port 2 TX/RX Positive Channel A	**TX_RXP_A_2**	AIO	Port 2 Channel A positive signal of differential pair
Ethernet Port 2 TX/RX Negative Channel A	**TX_RXN_A_2**	AIO	Port 2 Channel A negative signal of differential pair
Ethernet Port 2 TX/RX Positive Channel B	**TX_RXP_B_2**	AIO	Port 2 Channel B positive signal of differential pair
Ethernet Port 2 TX/RX Negative Channel B	**TX_RXN_B_2**	AIO	Port 2 Channel B negative signal of differential pair
Ethernet Port 2 TX/RX Positive Channel C	**TX_RXP_C_2**	AIO	Port 2 Channel C positive signal of differential pair
Ethernet Port 2 TX/RX Negative Channel C	**TX_RXN_C_2**	AIO	Port 2 Channel C negative signal of differential pair
Ethernet Port 2 TX/RX Positive Channel D	**TX_RXP_D_2**	AIO	Port 2 Channel D positive signal of differential pair
Ethernet Port 2 TX/RX Negative Channel D	**TX_RXN_D_2**	AIO	Port 2 Channel D negative signal of differential pair
Ethernet Port 3 TX/RX Positive Channel A	**TX_RXP_A_3**	AIO	Port 3 Channel A positive signal of differential pair
Ethernet Port 3 TX/RX Negative Channel A	**TX_RXN_A_3**	AIO	Port 3 Channel A negative signal of differential pair
Ethernet Port 3 TX/RX Positive Channel B	**TX_RXP_B_3**	AIO	Port 3 Channel B positive signal of differential pair
Ethernet Port 3 TX/RX Negative Channel B	**TX_RXN_B_3**	AIO	Port 3 Channel B negative signal of differential pair
Ethernet Port 3 TX/RX Positive Channel C	**TX_RXP_C_3**	AIO	Port 3 Channel C positive signal of differential pair

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TABLE 3-2: ETHERNET MEDIA INTERFACE PINS (CONTINUED)

Name	Symbol	Buffer Type	Description
Ethernet Port 3 TX/RX Negative Channel C	**TX_RXN_C_3**	AIO	Port 3 Channel C negative signal of differential pair
Ethernet Port 3 TX/RX Positive Channel D	**TX_RXP_D_3**	AIO	Port 3 Channel D positive signal of differential pair
Ethernet Port 3 TX/RX Negative Channel D	**TX_RXN_D_3**	AIO	Port 3 Channel D negative signal of differential pair

TABLE 3-3: QSGMII INTERFACE PINS

Name	Symbol	Buffer Type	Description
QSGMII Transmitter Output Positive	**QSGMII_TXP**	AO	QSGMII PHY to MAC positive signal of differential pair
QSGMII Transmitter Output Negative	**QSGMII_TXN**	AO	QSGMII PHY to MAC negative signal of differential pair
QSGMII Receiver Input Positive	**QSGMII_RXP**	AI	QSGMII MAC to PHY positive signal of differential pair
QSGMII Receiver Input Negative	**QSGMII_RXN**	AI	QSGMII MAC to PHY negative signal of differential pair
QSGMII External Reference Clock Input Positive	**REF_PAD_CLK_P**	LVDS2	Positive signal of differential pair. For Serializer/Deserializer (SerDes) testing. Refer to **REF_CLK_SEL[1:0]** for additional information.
QSGMII External Reference Clock Input Negative	**REF_PAD_CLK_M**	LVDS2	Negative signal of differential pair. For SerDes testing. Refer to **REF_CLK_SEL[1:0]** for additional information.

TABLE 3-4: SYSTEM CLOCK PINS

Name	Symbol	Buffer Type	Description
Crystal Input / System Reference Clock Input	**XI**	ICLK	When using a 25 MHz crystal, this input is connected to one lead of the crystal. Refer to **REF_CLK_SEL[1:0]** for additional information. When using a 25 MHz system reference clock, this is the input from the external 25 MHz oscillator.
Crystal Output	**XO**	OCLK	When using a 25 MHz crystal, this output is connected to one lead of the crystal. Refer to **REF_CLK_SEL[1:0]** for additional information. When using a 25 MHz system reference clock source, this pin is not connected.
System Reference Clock Input Positive	**CK125_REF_INP**	LVDS1	Positive signal of differential pair. When using a 125 MHz system reference clock source, this is connected to the external 125 MHz oscillator. Refer to **REF_CLK_SEL[1:0]** for additional information.
System Reference Clock Input Negative	**CK125_REF_INM**	LVDS1	Negative signal of differential pair. When using a 125 MHz system reference clock source, this is connected to the external 125 MHz oscillator. Refer to **REF_CLK_SEL[1:0]** for additional information.
System Clock Output	**CK25OUT**	OCLK	Buffered copy of internal 25 MHz reference clock. This output clock is powered by **VDDAH**.

TABLE 3-5: MISCELLANEOUS PINS

Name	Symbol	Buffer Type	Description
Management Interface Data	**MDIO**	VIS/ VO12 VOD12	PHY Management data interface. **Note:** An external pull-up resistor to **VDDIO** in the range of 1.0 kΩ to 4.7 kΩ is required (1.0 kΩ for high-speed MDIO operation). The buffer type (push-pull or open-drain/open-source) depends on the setting of the MDIO Buffer Type bit in the Output Control register, as well as the disable_mdo_drv bit in each port's direct register 17. See Section 5.14.1, High-Speed MDIO Operation for additional details.
Management Interface Clock	**MDC**	VIS	PHY Management clock input.
PHY Interrupt	**INT_N**	VO12/ VOD12 (PU)	Programmable interrupt output. The buffer type (push-pull or open-drain) depends on the setting of the INT Buffer Type bit in the Output Control register and defaults to open-drain. The polarity depends on the setting of the Intr Polarity Invert bit in the Control register and defaults to active low.
Start of Frame Ports 3-0	**SOF[3:0]**	SRL	RX and TX Start of Frame indicator. A pulse indicates Start of Frame is detected on the selected transmit or receive port. These pins can be configured via the GPIO SOF Select register. This pin is shared with other functions.

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TABLE 3-5: MISCELLANEOUS PINS (CONTINUED)

<table>
<tr><th>Name</th><th>Symbol</th><th>Buffer Type</th><th>Description</th></tr>
<tr><td>General Purpose I/O</td><td>GPIO[23:0]</td><td>VIS/VO12/ VOD12/ SRL (PU)</td><td>General purpose I/O.

These I/Os are shared with various other functions. Buffer type and alternate function selection is configured via GPIO registers.
<table>
<tr><th rowspan="2">Symbol</th><th colspan="2">Buffer Type</th><th rowspan="2">Description</th></tr>
<tr><th>VIS/ VO12/ VOD12 (PU)</th><th>SRL (PU)</th></tr>
<tr><td>GPIO[0:2]</td><td></td><td>X</td><td>with internal 50 ohm termination</td></tr>
<tr><td>GPIO[3:6]</td><td>X</td><td></td><td></td></tr>
<tr><td>GPIO[7:10]</td><td></td><td>X</td><td>with internal 50 ohm termination</td></tr>
<tr><td>GPIO[11:14]</td><td>X</td><td></td><td></td></tr>
<tr><td>GPIO[15:16]</td><td></td><td>X</td><td>with internal 50 ohm termination</td></tr>
<tr><td>GPIO[17:20]</td><td>X</td><td></td><td></td></tr>
<tr><td>GPIO[21]</td><td></td><td>X</td><td>with internal 50 ohm termination</td></tr>
<tr><td>GPIO[22]</td><td>X</td><td></td><td></td></tr>
<tr><td>GPIO[23]</td><td></td><td>X</td><td>with internal 50 ohm termination</td></tr>
</table></td></tr>
<tr><td>System Reset</td><td>RESET_N</td><td>VIS (PU)</td><td>Chip reset (active low).

At power-up, RESET_N must not be de-asserted until all power and clocks have been stable for the specified minimum duration.

Hardware pin configurations are strapped-in at the de-assertion (rising edge) of RESET_N. See the Configuration Strap Input Pins section for details.</td></tr>
<tr><td>Port 0 LED 1</td><td>PORT0LED1</td><td>VO12/ VOD12/ VOS12</td><td>Programmable Port 0 LED 1 output.

The polarity of this pin depends on the PORT0_LED1_POL configuration strap which is shared with this pin.</td></tr>
<tr><td>Port 0 LED 2</td><td>PORT0LED2</td><td>VO12/ VOD12/ VOS12</td><td>Programmable Port 0 LED 2 output.

The polarity of this pin depends on the PORT0_LED2_POL configuration strap which is shared with this pin.</td></tr>
<tr><td>Port 1 LED 1</td><td>PORT1LED1</td><td>VO12/ VOD12/ VOS12</td><td>Programmable Port 1 LED 1 output.

The polarity of this pin depends on the PORT1_LED1_POL configuration strap which is shared with this pin.</td></tr>
<tr><td>Port 1 LED 2</td><td>PORT1LED2</td><td>VO12/ VOD12/ VOS12</td><td>Programmable Port 1 LED 2 output.

The polarity of this pin depends on the PORT1_LED2_POL configuration strap which is shared with this pin.</td></tr>
<tr><td>Port 2 LED 1</td><td>PORT2LED1</td><td>VO12/ VOD12/ VOS12</td><td>Programmable Port 2 LED 1 output.

The polarity of this pin depends on the PORT2_LED1_POL configuration strap which is shared with this pin.</td></tr>
</table>

TABLE 3-5: MISCELLANEOUS PINS (CONTINUED)

Name	Symbol	Buffer Type	Description
Port 2 LED 2	**PORT2LED2**	VO12/ VOD12/ VOS12	Programmable Port 2 LED 2 output. The polarity of this pin depends on the **PORT2_LED2_POL** configuration strap which is shared with this pin.
Port 3 LED 1	**PORT3LED1**	VO12/ VOD12/ VOS12	Programmable Port 3 LED 1 output. The polarity of this pin depends on the **PORT3_LED1_POL** configuration strap which is shared with this pin.
Port 3 LED 2	**PORT3LED2**	VO12/ VOD12/ VOS12	Programmable Port 3 LED 2 output. The polarity of this pin depends on the **PORT3_LED2_POL** configuration strap which is shared with this pin.
Coma Mode Control	**COMA_MODE**	VIS (PU)	Drive high to activate Coma mode. After all ports are configured, drive low to enable normal operation. Hold low to disable this feature.
Reference Clock Select	**REF_CLK_SEL[1:0]**	VIS	These pins control reference clock selection of the System PLL and QSGMII SerDes MPLL. **REF_CLK_SEL[1:0]** **00:** SYSPLL Reference 25 MHz from **XI/XO** QSGMII Reference 25 MHz from **XI/XO** **01:** RESERVED **10:** SYSPLL Reference 25 MHz from **CK125_REF_INP/M** QSGMII Reference 125 MHz from **CK125_REF_INP/M** **11:** RESERVED **Note:** These are live pins, not configuration straps, and must be permanently tied high/low. **Note:** **XI/XO** can be a 25 MHz crystal or a 25 MHz external clock. **CK125_REF_INP/M** is a 125 MHz external clock.
System Clock Output Enable	**CK25OUT_EN**	VIS	**CK25OUT** enable/disable: **0:** Disabled **1:** Enabled **Note:** This is a live pin, not a configuration strap.
QSGMII SerDes Voltage Regulator Bypass	**VREG_BYPASS**	VIS	QSGMII SerDes voltage regulator bypass: **0:** SerDes powered from internal 3.3V to 2.5V regulator (regulator in use) **1:** SerDes powered directly from 2.5V (regulator bypassed) **Note:** This pin must be permanently tied high/low.
LDO Controller Output	**LDO_O**	AO	On-chip +1.1V LDO controller output. This functionality has been defeatured. The pin should be left unconnected. Please refer to the errata for further details.
SerDes Bias Resistor	**RES_REF**	AI	This pin must be connected to ground through a 200Ω 1% 100 ppm/°C resistor.
PHY Bias Resistor	**ISET**	AI	This pin must be connected to ground through a 6.04 kΩ 1% resistor.
Test Mode	**TEST_MODE**	VIS	For normal operation, this pin must be pulled-down to ground.
No Connect	**NC**	-	For normal operation, this pin must be left unconnected.

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TABLE 3-6: JTAG PINS

Name	Symbol	Buffer Type	Description
JTAG Mux Select	**TMS**	SRL	JTAG test mode select
JTAG Clock	**TCK**	SRL	JTAG test clock
JTAG Data Input	**TDI**	SRL	JTAG data input
JTAG Data Output	**TDO**	SRL	JTAG data output

TABLE 3-7: CONFIGURATION STRAP INPUT PINS

Name	Symbol	Buffer Type	Description
PHY Base Address Configuration Straps	**PHYAD[4:0]**	VIS	Configures the PHY Management base address, used with MDIO bus transactions. The PHY base address, **PHYAD[4:0]**, is sampled and latched at power-up/reset and is configurable to any value from 0 to 1Fh. Each PHY address bit is configured as follows: Pulled-up = 1 Pulled-down = 0 The addresses of each of the 4 PHYs are the base value, as defined by **PHYAD[4:0]**, plus offsets of 0, 1, 2 and 3. Refer to Section 3.3.2, "PHY Address (PHYAD[4:0])" for additional information. **Note:** **PHYAD[4:0]** must never be greater than 'h1C.
LED Polarity Configuration Straps	**PORT0_LED1_POL** **PORT0_LED2_POL** **PORT1_LED1_POL** **PORT1_LED2_POL** **PORT2_LED1_POL** **PORT2_LED2_POL** **PORT3_LED1_POL** **PORT3_LED2_POL**	VIS	Configures LED polarity as Active High or Active Low. Since the LED pins are shared with configuration straps, the default polarity of the LED pins is determined during strap loading. If the strap value on a pin is a 0, the LED is set as active high (**PORTx_LEDy_POL** = 1), since it is assumed that a LED to ground is used as the pull-down. **Note:** When using a LED as a pull-down strap, an external supplemental pull-down resistor may be needed to ensure a valid low level. If the strap value on a pin is 1, the LED is set as active low (**PORTx_LEDy_POL** = 0), since it is assumed that a LED to **VDDIO** is used as the pull-up. Refer to Section 3.3.5, "LED Polarity (PORT[3:0]_LED[2:1]_POL)" for additional information.
Device Mode Configuration Straps	**MODE_SEL[4:0]**	VIS	Configures the specific functional mode of all PHYs. The **MODE[4:0]** configuration straps are sampled and latched at power-up/reset and are defined in Section 3.3.1, "Device Mode Select (MODE_SEL[4:0])".

TABLE 3-7: CONFIGURATION STRAP INPUT PINS (CONTINUED)

Name	Symbol	Buffer Type	Description
PHY Broadcast Mode Configuration Strap	**ALLPHYAD**	VIS	Configures the default support for PHY Broadcast access using PHY Address 0. The **ALLPHYAD** configuration strap is sampled and latched at power-up/reset and are defined as follows: **0:** Enable PHY Broadcast accesses by default **1:** Disable PHY Broadcast accesses by default Refer to Section 3.3.3, "All PHYs Address (ALLPHYAD)" for additional information.
LED Mode Configuration Strap	**LED_MODE**	VIS	Configures the device's LED behavior as Individual or Tri-Color. All 8 LEDs are configured with identical behavior. The **LED_MODE** configuration strap is sampled and latched at power-up/reset and is defined as follows: **0:** Tri-color-LED mode **1:** Individual-LED mode Refer to Section 3.3.4, "LED Mode Select (LED_MODE)" for additional information.

TABLE 3-8: POWER AND GROUND PINS

Name	Symbol	Buffer Type	Description
+2.5/3.3V Analog I/O Power Supply	**VDDAH** **VDDAH_P[3:0]** **VDDAH_SERDES** **VDDAH_PLL_PTP** **VDDAH_ABPVT**	P	+2.5/3.3V analog I/O power supply
+2.5/3.3V Analog Power Supply	**VDD33REF**	P	+2.5/3.3V analog power supply
+1.21V Analog Power Supply	**VDDAL_ADC_A_P[3:0]** **VDDAL_ADC_B_P[3:0]** **VDDAL_ADC_C_P[3:0]** **VDDAL_ADC_D_P[3:0]** **VDDAL_PLL** **VDDAL_SERDES** **VDDTXL_SERDES** **VDDAL_CK125**	P	+1.21V analog power supply
+3.3/2.5/1.8V Variable I/O Power Supply Input	**VDDIO** **VDDIO_1**	P	+3.3/2.5/1.8V variable I/O digital power supply input
+1.21V Digital Core Power Supply Input	**VDDCORE**	P	+1.21V digital core power supply input
Paddle Ground	**P_VSS**	GND	Common ground. This exposed paddle must be connected to the ground plane with a via array.
Ground	**VSS_CK125**	GND	Ground

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3.3 Configuration Straps

Configuration straps allow various features of the device to be automatically configured to user defined values. Configuration straps are latched upon the release of pin reset (**RESET_N**). Configuration straps do not include internal resistors and require the use of external resistors.

Note:	The system designer must ensure that configuration strap pins meet timing requirements. If configuration strap pins are not at the correct voltage level prior to being latched, the device may capture incorrect strap values.

Note:	When externally pulling configuration straps high, the strap must be tied to **VDDIO**.

APPLICATION NOTE: All straps must be pulled-up or pulled-down externally on the PCB to enable the desired operational state.

3.3.1 DEVICE MODE SELECT (MODE_SEL[4:0])

The **MODE_SEL[4:0]** configuration straps select the device mode as follows:

Note:	1000BT Half Duplex is not advertised in any of the below device modes.

Note:	When no strap-based configured is wanted, it is recommended to set **MODE_SEL[4:0]** to either 0x18 (single-port system) or 0x19 (multi-port system). Both values enable 1000FD 100FD/HD 10FD/HD with EEE.

TABLE 3-9: DEVICE MODE SELECTIONS (PRELIMINARY)

Test Modes	
MODE_SEL [4:0]	**Mode**
00010	RESERVED
00011	RESERVED
00100	RESERVED
00101	RESERVED
00110	RESERVED
00111	RESERVED
Functional Modes	
Power Down	
01000	Software Power Down PLL Enabled
01001	RESERVED
Auto-Negotiation Disabled, Auto MDIX Disabled, EEE Disabled	
01010	1000FD Master
01011	100FD
01100	100HD

Legend:

1000FD = 1000BASE-T Full Duplex
100FD = 100BASE-TX Full Duplex
100HD = 100BASE-TX Half Duplex
10FD = 10BASE-T Full Duplex
10HD = 10BASE-T Half Duplex
“X” means “is advertised by auto-negotiation” (for example 10BT FD and 10BT HD are both available auto-negotiation results when MODE_SEL = 10000).

TABLE 3-9: DEVICE MODE SELECTIONS (PRELIMINARY) (CONTINUED)

Auto-Negotiation Enabled, Auto MDIX Enabled, EEE Disabled, Asym and Sym Pause												
		Auto-Negotiation Advertisement									10BT cat3/5	AMDIX
		1000BT			100BT			10BT		Asym / Sym Pause		
		FD	Single / Multi	EEE	FD	HD	EEE	FD	HD			
10000	1000FD Single Port 100FD/HD 10FD/HD	X	S		X	X		X	X	X	cat3	X
10001	1000FD Multi Port 100FD/HD 10FD/HD	X	M		X	X		X	X	X	cat3	X
10010	1000FD Single Port	X	S							X	N/A	X
10011	1000FD Multi Port	X	M							X	N/A	X
10100	100FD/HD				X	X				X	N/A	X
10101	100FD				X					X	N/A	X
10110	100HD					X				X	N/A	X
10111	100FD/HD 10FD/HD				X	X		X	X	X	cat3	X
Auto-Negotiation Enabled, Auto MDIX Enabled, EEE Enabled, Asym and Sym Pause												
		Auto-Negotiation Advertisement									10BT cat3/5	AMDIX
		1000BT			100BT			10BT		Asym / Sym Pause		
		FD	Single / Multi	EEE	FD	HD	EEE	FD	HD			
11000	1000FD Single Port 100FD/HD 10FD/HD	X	S	X	X	X	X	X	X	X	cat5	X
11001	1000FD Multi Port 100FD/HD 10FD/HD	X	M	X	X	X	X	X	X	X	cat5	X
11010	1000FD Single Port	X	S	X						X	N/A	X
11011	1000FD Multi Port	X	M	X						X	N/A	X
11100	100FD/HD				X	X	X			X	N/A	X
11101	100FD				X		X			X	N/A	X
11111	100FD/HD 10FD/HD				X	X	X	X	X	X	cat5	X
RESERVED												
00000	RESERVED											
00001	RESERVED											
01101	RESERVED											
01110	RESERVED											

Legend:

1000FD = 1000BASE-T Full Duplex
100FD = 100BASE-TX Full Duplex
100HD = 100BASE-TX Half Duplex
10FD = 10BASE-T Full Duplex
10HD = 10BASE-T Half Duplex
“X” means “is advertised by auto-negotiation” (for example 10BT FD and 10BT HD are both available auto-negotiation results when MODE_SEL = 10000).

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TABLE 3-9: DEVICE MODE SELECTIONS (PRELIMINARY) (CONTINUED)

01111	RESERVED
11110	RESERVED

Legend:

1000FD = 1000BASE-T Full Duplex
100FD = 100BASE-TX Full Duplex
100HD = 100BASE-TX Half Duplex
10FD = 10BASE-T Full Duplex
10HD = 10BASE-T Half Duplex
"X" means "is advertised by auto-negotiation" (for example 10BT FD and 10BT HD are both available auto-negotiation results when MODE_SEL = 10000).

3.3.2 PHY ADDRESS (PHYAD[4:0])

The **PHYAD[4:0]** configuration straps set the base value of the PHY's management address. The addresses of each of the 4 PHYs are the base value, as defined by **PHYAD[4:0]**, plus offsets of 0, 1, 2 and 3.

3.3.3 ALL PHYs ADDRESS (ALLPHYAD)

The **ALLPHYAD** configuration strap sets the default of the All-PHYAD Enable bit in the Common Control register which enables (pulled-down) or disables (pulled-up) the PHY's ability to respond to PHY Address 0 as well as it's assigned PHY address.

Note: This strap input is inverted compared to the register bit.

3.3.4 LED MODE SELECT (LED_MODE)

The **LED_MODE** configuration strap selects between Individual-LED (pulled-up) or Tri-color-LED (pulled-down) modes. All 8 LEDs are configured with identical behavior. The **LED_MODE** configuration strap is sampled and latched at power-up/reset and is defined as follows:

0: Tri-color-LED mode

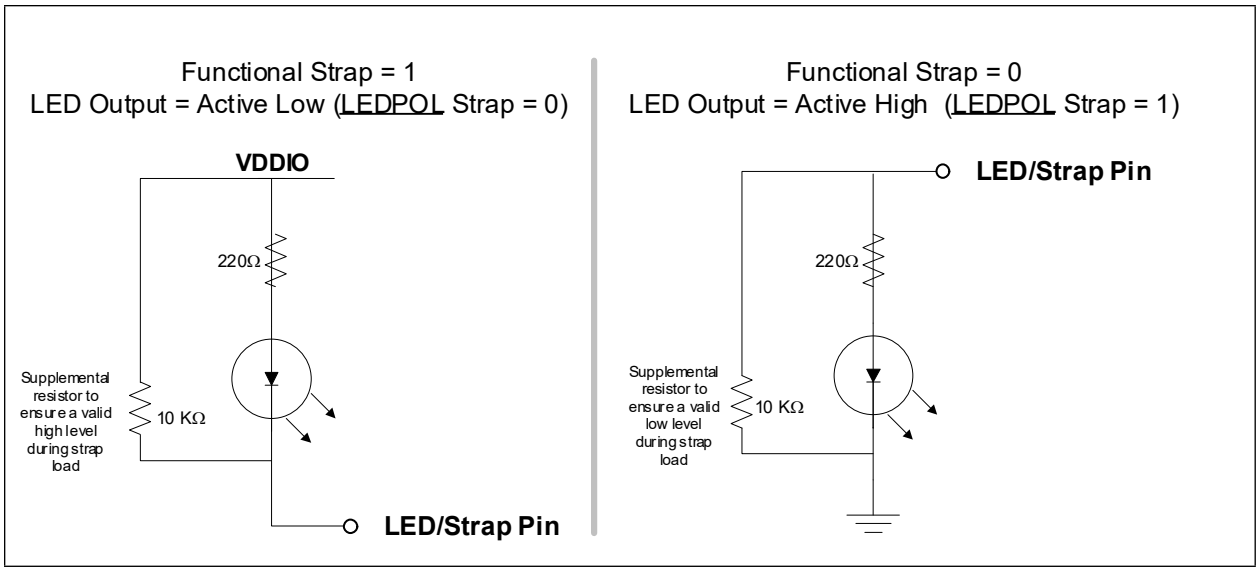
1: Individual-LED mode

LED operation is described in Section 5.17, "LEDs".

3.3.5 LED POLARITY (PORT[3:0]_LED[2:1]_POL)

The **PORT[3:0]_LED[2:1]_POL** configuration straps set the default polarity of the LED pins. When a LED pin is used as a function mode strap (for example a PHY address bit), the default LED pin polarity is automatically selected based on the inverse of the strap value. A LED, via a resistor, is then used as a pull-up or pull-down. This is shown in Figure 3-2.

FIGURE 3-2: STRAP ON LED WITH POLARITY



LED operation is described in Section 5.17, "LEDs".

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4.0 DEVICE CONNECTIONS

The following example device connection information and diagrams are included in this section:

- Voltage Regulator and Power Connections
- QSGMII MAC Interface
- Ethernet Media Interface

4.1 Voltage Regulator and Power Connections

The LAN8804 has an integrated LDO controller. This controller has been defeatured. Please refer to the errata for further details.

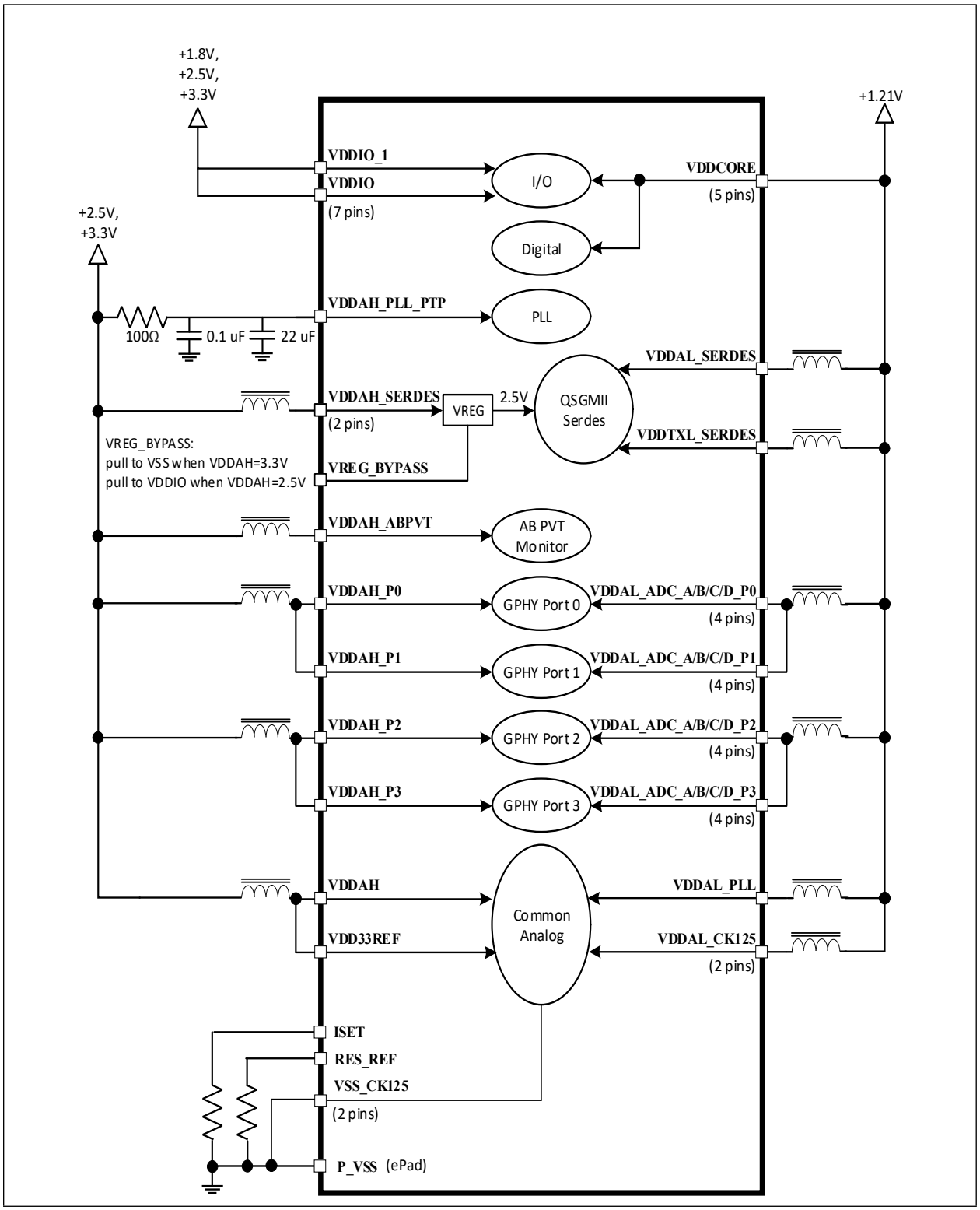
4.1.1 LDO DISABLE

The LDO controller is enabled by default. The LDO has been defeatured and **LDO_O** should be left disconnected. Microchip recommends disabling the LDO output by setting the active low LDO enable bit in the Analog Control Register 11. An external source of 1.21V is required for operation.

4.1.2 POWER CONNECTIONS

Figure 4-1 illustrates the device power connections.

FIGURE 4-1: POWER CONNECTIONS

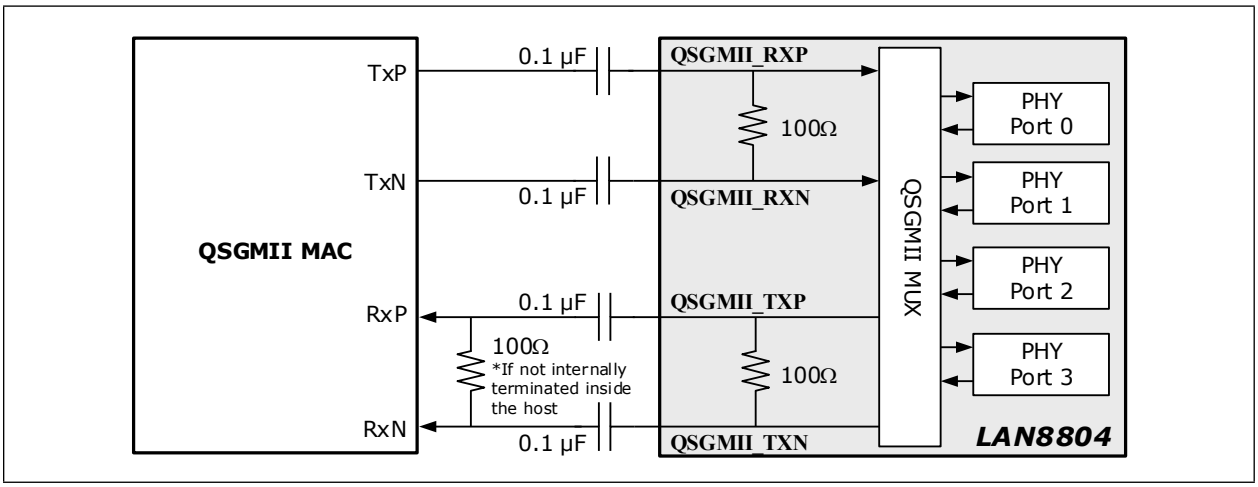


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4.2 QSGMII MAC Interface

Figure 4-2 illustrates the device QSGMII MAC interface connections.

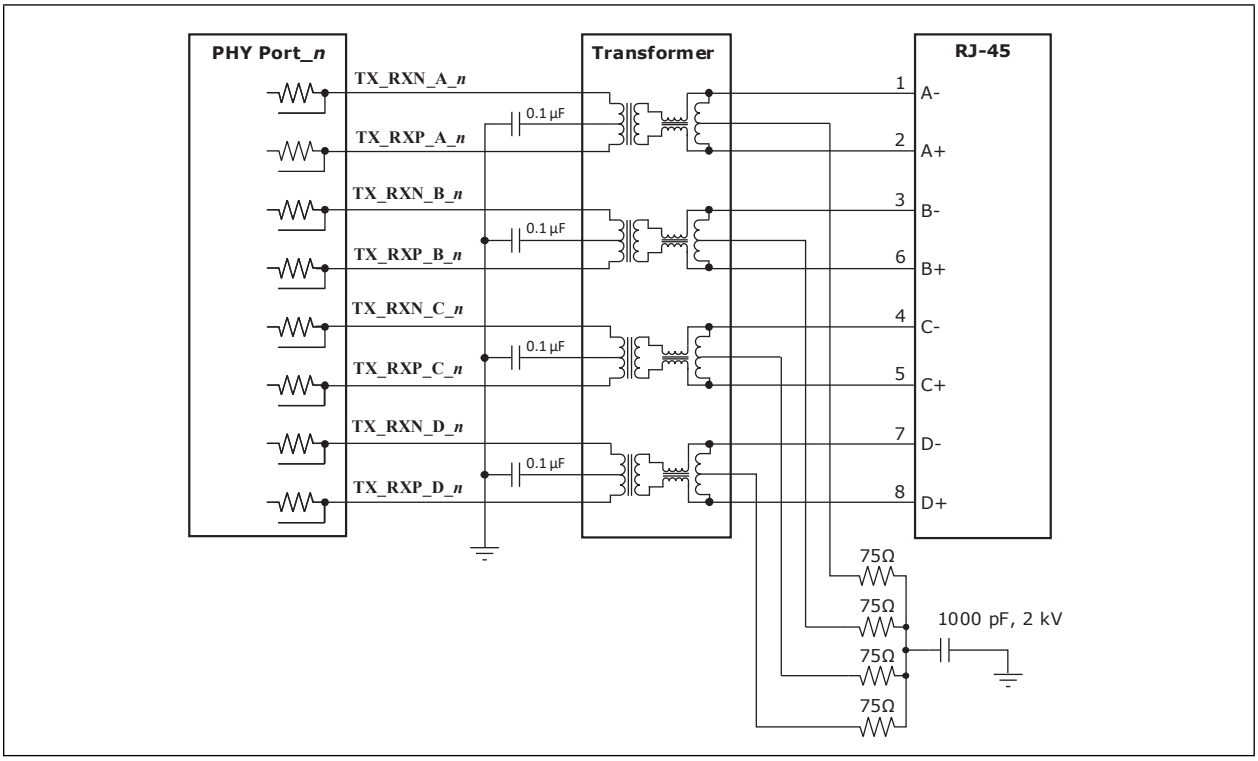
FIGURE 4-2: QSGMII MAC INTERFACE CONNECTIONS



4.3 Ethernet Media Interface

Figure 4-3 illustrates the device Ethernet media interface connections.

FIGURE 4-3: ETHERNET MEDIA INTERFACE CONNECTIONS



Note: The device supports integrated connector magnetics with ganged center taps.

5.0 FUNCTIONAL DESCRIPTIONS

This section provides additional details of the major features supported by the LAN8804:

- 10BASE-T/100BASE-TX Transceiver
- 1000BASE-T Transceiver
- Auto MDI/MDIX (Pair-Swap)
- Alignment and Polarity Detection/Correction
- Wave Shaping, Slew-Rate Control, and Partial Response
- Auto-Negotiation
- LinkMD Cable Diagnostics
- Energy Efficient Ethernet (EEE)
- IEEE 802.3-2018 Frame Preemption
- Start of Frame Indication
- Signal Quality Index
- Loopbacks
- QSGMII
- MIIM (MDIO) Interface
- Interrupts
- GPIOs
- LEDs
- Coma Mode
- Power Management
- PLL/Clocks and Resets
- JTAG

5.1 10BASE-T/100BASE-TX Transceiver

5.1.1 100BASE-TX TRANSMIT

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT-3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125 MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT-3 current output. The output current is set by an external 6.04 kΩ 1% resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4 ns and complies with the ANSI TP-PMD standard regarding amplitude balance, and overshoot. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

5.1.2 100BASE-TX RECEIVE

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT-3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Because the amplitude loss and phase distortion are a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC-restoration and data-conversion block. The DC-restoration circuit compensates for the effect of baseline wander and improves the dynamic range. The differential data conversion circuit converts the MLT-3 format back to NRZI. The slicing threshold is also adaptive.

The clock-recovery circuit extracts the 125 MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII/GMII or Reduced Gigabit Media Independent Interface format and provided as the input data to the MAC.

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5.1.3 SCRAMBLER/DE-SCRAMBLER (100BASE-TX ONLY)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander. Transmitted data is scrambled using an 11-bit wide Linear Feedback Shift Register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence, then the receiver de-scrambles the incoming data stream using the same sequence as at the transmitter.

5.1.4 10BASE-T TRANSMIT

The 10BASE-T output drivers are incorporated into the 100BASE-TX drivers to allow for transmission with the same magnetic. The drivers perform internal wave-shaping and pre-emphasis, and output signals with typical amplitude of 2.5V peak for standard 10BASE-T mode and 1.75V peak for energy-efficient 10BASE-Te mode. The 10BASE-T/ 10BASE-Te signals have harmonic contents that are at least 31 dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

5.1.5 10BASE-T RECEIVE

On the receive side, input buffer and level-detecting squelch circuits are used. A differential input receiver circuit and a Phase-Locked Loop (PLL) perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 300 mV or with short pulse widths to prevent noises at the receive inputs from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the device decodes a data frame. The receiver clock is maintained active during idle periods between receiving data frames.

The device removes all 7 bytes of the preamble and presents the received frame starting with the Start of Frame Delimiter (SFD) to the MAC.

Auto-polarity correction is provided for the receiving differential pair to automatically swap and fix the incorrect ± polarity wiring in the cabling.

5.2 1000BASE-T Transceiver

The 1000BASE-T transceiver is based on a mixed-signal/digital-signal processing (DSP) architecture, which includes the analog front-end, digital channel equalizers, trellis encoders/decoders, echo cancelers, cross-talk cancelers, precision clock recovery scheme, and power-efficient line drivers.

5.2.1 ANALOG ECHO-CANCELLATION CIRCUIT

In 1000BASE-T mode, the analog echo-cancellation circuit helps to reduce the near-end echo. This analog hybrid circuit relieves the burden of the ADC and the adaptive equalizer.

This circuit is disabled in 10BASE-T/100BASE-TX mode.

5.2.2 AUTOMATIC GAIN CONTROL (AGC)

In 1000BASE-T mode, the AGC circuit provides initial gain adjustment to boost up the signal level. This pre-conditioning circuit is used to improve the signal-to-noise ratio of the receive signal.

5.2.3 ANALOG-TO-DIGITAL CONVERTER (ADC)

In 1000BASE-T mode, the ADC digitizes the incoming signal. ADC performance is essential to the overall performance of the transceiver.

This circuit is disabled in 10BASE-T/100BASE-TX mode.

5.2.4 TIMING RECOVERY CIRCUIT

In 1000BASE-T mode, the mixed-signal clock recovery circuit together with the digital PLL is used to recover and track the incoming timing information from the received data. The digital PLL has very low long-term jitter to maximize the signal-to-noise ratio of the receive signal.

The 1000BASE-T slave PHY must transmit the exact receive clock frequency recovered from the received data back to the 1000BASE-T master PHY. Otherwise, the master and slave will not be synchronized after long transmission. This also helps to facilitate echo cancellation and NEXT removal.

5.2.5 ADAPTIVE EQUALIZER

In 1000BASE-T mode, the adaptive equalizer provides the following functions:

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- Detection for partial response signaling
- Removal of NEXT and ECHO noise
- Channel equalization

Signal quality is degraded by residual echo that is not removed by the analog hybrid because of impedance mismatch. The device uses a digital echo canceler to further reduce echo components on the receive signal.

In 1000BASE-T mode, data transmission and reception occurs simultaneously on all four pairs of wires (four channels). This results in high-frequency cross-talk coming from adjacent wires. The device uses three NEXT cancelers on each receive channel to minimize the cross-talk induced by the other three channels.

In 10BASE-T/100BASE-TX mode, the adaptive equalizer needs only to remove the inter-symbol interference and recover the channel loss from the incoming data.

5.2.6 TRELLIS ENCODER AND DECODER

In 1000BASE-T mode, the transmitted 8-bit data is scrambled into 9-bit symbols and further encoded into 4D-PAM5 symbols. The initial scrambler seed is determined by the specific PHY address to reduce EMI when more than one device is used on the same board. On the receiving side, the idle stream is examined first. The scrambler seed, pair skew, pair order, and polarity must be resolved through the logic. The incoming 4D-PAM5 data is then converted into 9-bit symbols and de-scrambled into 8-bit data.

5.3 Auto MDI/MDIX (Pair-Swap)

The Automatic MDI/MDI-X feature eliminates the need to determine whether to use a straight cable or a crossover cable between the device and its link partner. This auto-sense function detects the MDI/MDI-X pair mapping from the link partner, and assigns the MDI/MDI-X pair mapping of the device accordingly.

Table 5-1 shows the device 10/100/1000 pin configuration assignments for MDI/MDI-X pin mapping.

TABLE 5-1: MDI/MDI-X PIN MAPPING

Pin (RJ-45 Pair)	MDI			MDI-X		
	1000BASE-T	100BASE-T	10BASE-T	1000BASE-T	100BASE-T	10BASE-T
TX_RXP/N_A_*x* (1, 2)	A+/-	TX+/-	TX+/-	B+/-	RX+/-	RX+/-
TX_RXP/N_B_*x* (3, 6)	B+/-	RX+/-	RX+/-	A+/-	TX+/-	TX+/-
TX_RXP/N_C_*x* (4, 5)	C+/-	Not Used	Not Used	C+/- (Note 5-1)	Not Used	Not Used
TX_RXP/N_D_*x* (7, 8)	D+/-	Not Used	Not Used	D+/- (Note 5-1)	Not Used	Not Used

Note 5-1 Default value is shown in the table. C pair can be swapped with D pair via register settings.

Auto-MDIX detection is enabled in the device by default.

Auto-MDIX can be disabled by setting the swapoff bit in the Digital Debug Control 1 register. The MDI/MDI-X mode may then be manually selected by the mdi_set bit in the Digital Debug Control 1 register.

The Auto-MDIX status bits are located in the Digital AX/AN Status register.

An isolation transformer with symmetrical transmit and receive data paths is recommended to support Auto MDI/MDI-X.

5.4 Alignment and Polarity Detection/Correction

In 1000BASE-T mode, the device supports 50 ns ±10 ns difference in propagation delay between pairs of channels in accordance with the IEEE 802.3 standard, and automatically corrects the data skew so the corrected four pairs of data symbols are synchronized.

Additionally, the device detects and corrects polarity errors on all MDI pairs, a useful capability that exceeds the requirements of the standard. Polarity detection and correction applies to 10BASE-T and 1000BASE-T and is not required for 100BASE-TX.

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5.5 Wave Shaping, Slew-Rate Control, and Partial Response

In communication systems, signal transmission encoding methods are used to provide the noise-shaping feature and to minimize distortion and error in the transmission channel.

- For 1000BASE-T, a special partial-response signaling method is used to provide the band-limiting feature for the transmission path.
- For 100BASE-TX, a simple slew-rate control method is used to minimize EMI.
- For 10BASE-T, pre-emphasis is used to extend the signal quality through the cable.

5.6 Auto-Negotiation

The device conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3 Specification [1].

Auto-negotiation allows UTP link partners to select the highest common mode of operation.

During auto-negotiation, link partners advertise capabilities across the UTP link to each other, and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the operating mode.

The following list shows the speed and duplex operation mode from highest to lowest:

- Priority 1: 1000BASE-T, full-duplex
- Priority 2: 1000BASE-T, half-duplex (Note 5-2)
- Priority 3: 100BASE-TX, full-duplex
- Priority 4: 100BASE-TX, half-duplex
- Priority 5: 10BASE-T, full-duplex
- Priority 6: 10BASE-T, half-duplex

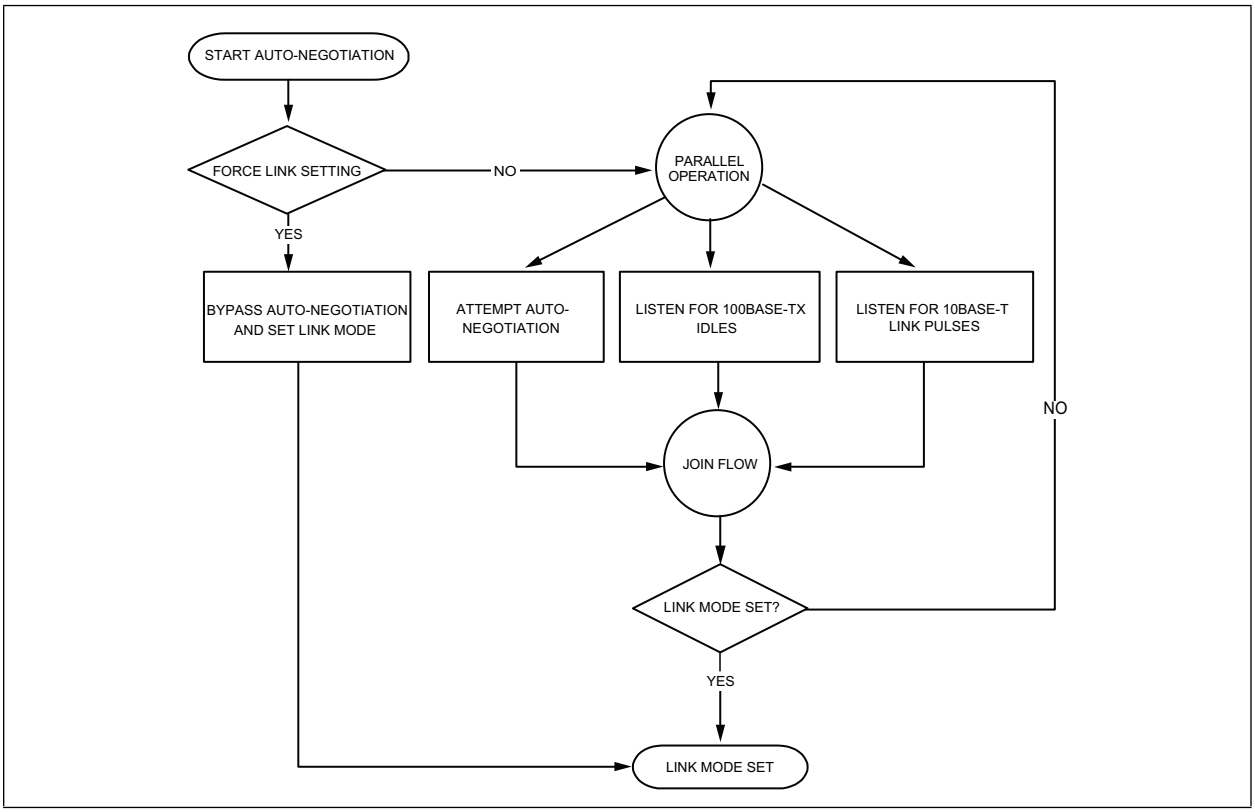
Note 5-2 The device does not support 1000BASE-T, half-duplex and may not be enabled to advertise such.

If auto-negotiation is not supported or the device's link partner is forced to bypass auto-negotiation for 10BASE-T and 100BASE-TX modes, the device sets its operating mode by observing the input signal at its receiver. This is known as parallel detection, and allows the device to establish a link by listening for a fixed signal protocol in the absence of the auto-negotiation advertisement protocol.

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The auto-negotiation link-up process is shown in Figure 5-1.

FIGURE 5-1: AUTO-NEGOTIATION FLOW CHART



For 1000BASE-T mode, auto-negotiation is required and always used to establish a link. During 1000BASE-T auto-negotiation, the master and slave configuration is first resolved between link partners. Then the link is established with the highest common capabilities between link partners.

Auto-negotiation is enabled by default after power-up or hardware reset. After that, auto-negotiation can be enabled or disabled through the Basic Control register, bit[12]. If auto-negotiation is disabled, the speed is set by the Basic Control register, bits[6, 13] and the duplex is set by the Basic Control register, bit[8].

If the speed is changed on the fly, the link goes down and either auto-negotiation and parallel detection initiate until a common speed between the device and its link partner is re-established for a link.

If the link is already established and there is no change of speed on the fly, the changes (for example, duplex and pause capabilities) will not take effect unless either auto-negotiation is restarted through the Basic Control register, bit[9], or a link-down to link-up transition occurs (that is, disconnecting and reconnecting the cable).

After auto-negotiation is completed, the link status is updated in the Basic Status register, bit[2], and the link partner capabilities are updated in Registers 5h, 6h, 8h, and Ah.

The auto-negotiation finite state machines use interval timers to manage the auto-negotiation process. The duration of these timers under normal operating conditions is summarized in Table 5-2.

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TABLE 5-2: AUTO-NEGOTIATION TIMERS

Auto-Negotiation Interval Timers	Time Duration
Transmit Burst Interval	16 ms
Transmit Pulse Interval	68 µs
FLP Detect Minimum Time	17.2 µs
FLP Detect Maximum Time	185 µs
Receive Minimum Burst Interval	6.8 ms
Receive Maximum Burst Interval	112 ms
Data Detect Minimum Interval	35.4 µs
Data Detect Maximum Interval	95 µs
Normal Link Pulse (NLP) Test Minimum Interval	4.5 ms
NLP Test Maximum Interval	30 ms
Link Loss Time	52 ms
Break Link Time	1480 ms
Parallel Detection Wait Time	830 ms
Link Enable Wait Time	1000 ms

5.6.1 AUTO-NEGOTIATION NEXT PAGE USAGE

The device supports “Next Page” capability which is used to negotiate Gigabit Ethernet and Energy Efficient Ethernet functionality as well as to support software controlled pages.

As described in IEEE 802.3 Annex 40C “Add-on interface for additional Next Pages”, the device will autonomously send and receive the Gigabit Ethernet and Energy Efficient Ethernet next pages and then optionally send and receive software controlled next pages.

Gigabit Ethernet next pages consist of one message and two unformatted pages. The message page contains an 8 as the message code. The first unformatted page contains the information from the Auto-Negotiation Master Slave Control register. The second unformatted page contains the Master-Slave Seed value used to resolve the Master-Slave selection. The result of the Gigabit Ethernet next pages exchange is stored in Auto-Negotiation Master Slave Status register.

Gigabit Ethernet next pages are always transmitted, regardless of the advertised settings in the Auto-Negotiation Master Slave Control register.

Energy Efficient Ethernet (EEE) next pages consist of one message and one unformatted page. The message page contains a 10 as the message code (this value can be overridden in the EEE Message Code register). The unformatted page contains the information from the EEE Advertisement register. The result of the Gigabit Ethernet next pages exchange is stored in EEE Link Partner Ability register.

EEE next pages are transmitted only if the advertised setting in the EEE Advertisement register is not zero.

APPLICATION NOTE: The Gigabit Ethernet and EEE next pages may be viewed in Auto-Negotiation Next Page RX register as they are exchanged.

Following the EEE next page exchange, software controlled next pages are exchanged when the Next Page bit in the Auto-Negotiation Advertisement register is set. Software controlled next page status is monitored via the Auto-Negotiation Expansion register and Auto-Negotiation Next Page RX register.

5.6.2 PARALLEL DETECT DUPLEX

Normally, and according to IEEE 802.3, when parallel detection is used to establish the link, the resulting operation is set to half duplex. An option exists to force this result to full duplex. This is enabled by setting the LP Force 100 FD Override and/or LP Force 10 FD Override bits in the Parallel Detect Full Duplex Override register.

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5.7 LinkMD Cable Diagnostics

The LinkMD function uses Time Domain Reflectometry (TDR) to analyze the cabling plant for common cabling problems, such as open circuits, short circuits, and impedance mismatches as well as the distance to the fault. Each of the four twisted pairs are tested separately.

LinkMD operates by sending a pulse of known amplitude and duration down the selected differential pair, then analyzing the polarity and shape of the reflected signal to determine the type of fault: open circuit for a positive/non-inverted amplitude reflection and short circuit for a negative/inverted amplitude reflection. The time duration for the reflected signal to return provides the approximate distance to the cabling fault. The LinkMD function processes this TDR information and presents it as a numerical value that can be translated to a cable distance.

LinkMD is initiated by accessing the Cable Diagnostic register. To test each individual cable pair, set the cable pair in the Cable Diagnostics Test Pair (VCT_PAIR[1:0]) field of the Cable Diagnostic register, along with setting the Cable Diagnostics Test Enable (VCT_EN) bit. The Cable Diagnostics Test Enable (VCT_EN) bit will self-clear when the test is concluded.

The test results (for the pair just tested) are available in the Cable Diagnostic register. With the bit[9:0] Definition (VCT_SEL[1:0]) field set to ‘0’, the Cable Diagnostics Status (VCT_ST[1:0]) field will indicate a Normal (properly terminated), Open or Short condition, or Failed test.

If the test result was Open or Short, the Cable Diagnostics Data or Threshold (VCT_DATA[7:0]) field indicates the distance to the fault in meters as approximately:

- distance to fault = (VCT_DATA - 22) * 4 / cable propagation velocity

This provides an accuracy of ± 2% to 3% for short and medium cables and ± 5% to 6% for long cables. Inaccuracy is due to cable pitch differences between cable manufacturers, where cable pitch is the number of wire twists per unit cable length.

Link MD supports diagnostic cable testing int he following three scenarios:

- LinkMD with No Link Partner
- LinkMD with Fully Passive Link Partner
- LinkMD with Partially Active Link Partner

5.7.1 LINKMD WITH NO LINK PARTNER

In this scenario, the remote end of the cable is unplugged.

Prior to running the cable diagnostics, perform a software reset via the Basic Control Register. After reset, the following must be configured:

- Auto Negotiation disabled via the Digital Debug Control 1 Register
- Auto MDI/MDI-X disabled via the Digital Debug Control 1 Register
- Full Duplex set via the Basic Control Register
- Link Speed set to 1000 Mbps via the Basic Control Register
- Master-Slave configuration set to Slave via the Auto Negotiation Master Slave Control Register

Wait 10 ms prior to testing the pairs.

In this scenario, for each of the four twisted pairs, LinkMD should only return Open or Short along with a distance.

- Open with “distance” providing the correct cable length indicates a good cable
- Short or Open with any other distance indicates a bad cable

After running the cable diagnostics, perform another software reset via the Basic Control Register

5.7.2 LINKMD WITH FULLY PASSIVE LINK PARTNER

In this scenario, the remote end of the cable is connected to a Link Partner. The Link Partner must be powered down or configured to be in the following passive state:

- Auto Negotiation disabled
- Auto MDI/MDI-X disabled

Prior to running the cable diagnostics, perform a software reset via the Basic Control Register. After reset, the following must be configured:

- Auto Negotiation disabled via the Digital Debug Control 1 Register

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- Auto MDI/MDI-X disabled via the Digital Debug Control 1 Register
- Full Duplex set via the Basic Control Register
- Link Speed set to 1000 Mbps via the Basic Control Register
- Master-Slave configuration set to Slave via the Auto Negotiation Master Slave Control Register

Wait 10 ms prior to testing the pairs.

In this scenario, for each of the four twisted pairs, LinkMD will return Open or Short along with a distance, or Normal.

- Normal indicates a good cable which is properly terminated at the Link Partner. Due to no TDR reflections, no cable distance is available with this result (VCT[7:0] is invalid).
- Open or Short indicates a bad cable or improper Link Partner termination. VCT[7:0] indicates the distance to the cable fault.

After running the cable diagnostics, perform another software reset via the Basic Control Register.

5.7.3 LINKMD WITH PARTIALLY ACTIVE LINK PARTNER

In this scenario, the remote end of the cable is connected to a Link Partner. The Link Partner is powered up and in the following state:

- Auto Negotiation may be enabled, disabled, or unknown
- Auto MDI/MDI-X is disabled, but we are able to selectively configure MDI or MDI-X, as required for the LinkMD tests

Prior to running the cable diagnostics, perform a software reset via the Basic Control Register. After reset, the following must be configured:

- Auto Negotiation disabled via the Digital Debug Control 1 Register
- Auto MDI/MDI-X disabled via the Digital Debug Control 1 Register
- Full Duplex set via the Basic Control Register
- Link Speed set to 1000 Mbps via the Basic Control Register
- Master-Slave configuration set to Slave via the Auto Negotiation Master Slave Control Register

Wait 10 ms prior to testing the pairs.

The LinkMD test is first run with the Link Partner in MDI mode on twisted pairs B, C, and D.

The LinkMD test is then run with the Link Partner in MDI-X mode on twisted pair A.

- Normal indicates a good cable which is properly terminated at the Link Partner. Due to no TDR reflections, no cable distance is available with this result (VCT[7:0] is invalid).
- Open or Short indicates a bad cable or improper Link Partner termination. VCT[7:0] indicates the distance to the cable fault.

After running the cable diagnostics, perform another software reset via the Basic Control Register.

APPLICATION NOTE: If the Cable Diagnostics Status (VCT_ST[1:0]) field indicates Failed, it is generally due to multiple pulses being received after sending out a single pulse. In this Partially Active test, the Link Partner is allowed to be in the Auto-Negotiation state, but if the Link Partner is mistakenly in forced 1000BASE-T or 100BASE-TX mode, the test will fail.

APPLICATION NOTE: Any signal received from a link partner will interfere with the TDR test. Energy detection must first be checked on each wire pair by using the procedure in Section 5.19.2, "Energy-Detect Power-Down Mode".

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5.8 Energy Efficient Ethernet (EEE)

The device implements Energy Efficient Ethernet (EEE) as described in IEEE Standard 802.3az. The specification is defined around an EEE-compliant MAC on the host side and an EEE-compliant link partner on the line side that support the special signaling associated with EEE. EEE saves power by keeping the AC signal on the copper Ethernet cable at approximately 0V peak-to-peak as often as possible during periods of no traffic activity, while maintaining the link-up status. This is referred to as Low Power Idle (LPI) mode or state.

As set by the **MODE_SEL[4:0]** configuration straps, the device has the EEE function enabled or disabled as the power-up default setting. The EEE function can be enabled or disabled by setting or clearing the following EEE advertisement bits in the EEE Advertisement register (MDIO Manageable Device (MMD) Address 7h, register 3Ch), followed by restarting auto-negotiation (writing a '1' to the Basic Control register, bit[9]):

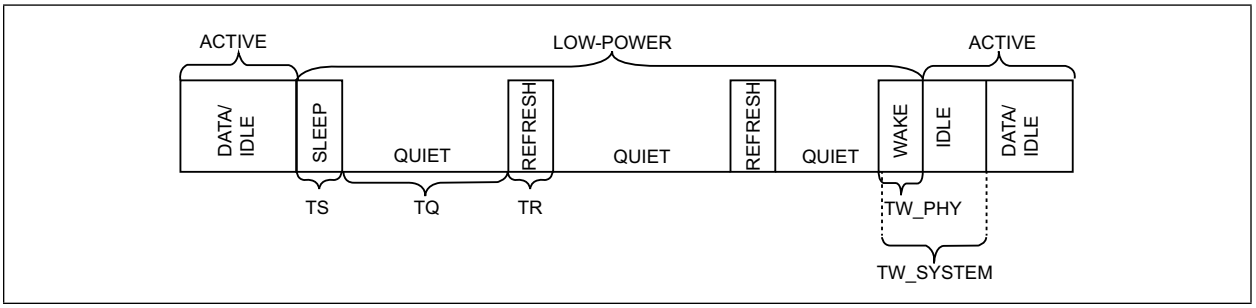
- 1000BASE-T EEE (bit[2]) = '0/1' // Disable/Enable 1000 Mbps EEE mode
- 100BASE-TX EEE (bit[1]) = '0/1' // Disable/Enable 100 Mbps EEE mode

During LPI mode, the copper link responds automatically when it receives traffic and resumes normal PHY operation immediately, without blockage of traffic or loss of packet. This involves exiting LPI mode and returning to normal 100/1000 Mbps operating mode. Wake-up times are <16 µs for 1000BASE-T and <30 µs for 100BASE-TX. The LPI state is controlled independently for transmit and receive paths, allowing the LPI state to be active (enabled) for:

- Transmit cable path only
- Receive cable path only
- Both transmit and receive cable paths

During LPI mode, refresh transmissions are used to maintain the link; power savings occur in quiet periods. Approximately every 20 to 22 milliseconds, a refresh transmission of 200 to 220 microseconds is sent to the link partner. The refresh transmissions and quiet periods are shown in Figure 5-2.

FIGURE 5-2: LPI MODE (REFRESH TRANSMISSIONS AND QUIET PERIODS)



5.8.1 TRANSMIT DIRECTION CONTROL (MAC-TO-PHY)

The PHY enters the LPI Sleep state for the transmit direction when the attached EEE-compliant MAC asserts the LPI opcode toward the PHY. The PHY remains in the transmit LPI Sleep state until the attached EEE-compliant MAC asserts a non-LPI opcode toward the PHY. While in the LPI Sleep state, the PHY will periodically send Refreshes to the EEE-compliant Link Partner to maintain the Link, clock recovery, etc.

5.8.2 RECEIVE DIRECTION CONTROL (PHY-TO-MAC)

The PHY enters LPI mode for the receive direction when it receives the /P/ code bit pattern (Sleep/Refresh) from its EEE-compliant Link Partner. The PHY will pass the Sleep Request to the attached EEE-compliant MAC. The PHY remains in the receive LPI Sleep state while it continues to receive Refreshes from its Link Partner, and it will continue to inform the attached EEE-compliant MAC that it is in the receive LPI Sleep state. When the PHY receives a non /P/ code bit pattern (non-refresh), it exits the receive LPI Sleep state and signals a normal frame or normal idle to the attached EEE-compliant MAC.

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5.9 IEEE 802.3-2018 Frame Preemption

IEEE Standard 802.3-2018 [1] specifies a method for interspersing express traffic by preempting the transmission of a normal packet, transmitting the express packet and then resuming the normal packet. The receiver likewise reassembles the fragmented normal packet.

The preemption and reassembly is performed using a newly defined mPacket format. This mPacket format starts with the normal preamble but supplements the normal Start of Frame Delimiter (SFD = 0xD5) with newly defined Start mPacket Delimiters (SMDs) of various values. Also added for certain mPackets is a fragment count octet.

If Frame Preemption is not in use, the SFD appears ahead of every Ethernet frame on the PHY port. If Frame Preemption is in use, one of several possible SMDs may appear in place of the SFD on the PHY ports. The SMD and SFD characters are passed transparently across QSGMII.

Section 5.10, "Start of Frame Indication" defines SOF pulse generation support for the SMDs.

APPLICATION NOTE: Preemption is not supported at 10 Mbps.

5.10 Start of Frame Indication

The device supports the generation of an SOF pulse for the receive and transmit paths. Four SOF outputs are available, each of which is configurable to be any of the eight available SOF pulses (TX SOF and RX SOF on each port). The SOF pulse is generated when the Start of Frame Delimiter (SFD octet 0xD5 immediately following the preamble) is detected by the PCS and can be output onto any enabled GPIO pin by setting the corresponding bits in the General Purpose IO Data Select 1 register (GPIO_DATA_SEL1) or the General Purpose IO Data Select 2 register (GPIO_DATA_SEL2). The SOF pulse is always active high. For details on SOF detection timing, refer to Section 6.6.8, "GPIO SOF Detection Timing".

Note:	The GPIO needs to be enabled and its direction set as an output via the General Purpose IO Enable register (GPIO_EN) and the General Purpose IO Direction register (GPIO_DIR). The GPIO Buffer Type (GPIO_BUF) field in the General Purpose IO Buffer Type register (GPIO_BUF) also applies.

The SOF pulse can also be configured to detect 802.3-2018 SMDs. When the SOF_preemption_enable bits in MMD2 register 75 are set to “10”, the SOF pulse is generated for any of the SMD values listed in 802.3-2018 *except* for the continuation frame: SMD-V (0x07), SMD-R (0x19), SMD-E (0xD5) and SMD-S[0,1,2,3] (0xE6, 0x4C, 0x7F or 0xB3). When the SOF_preemption_enable bits are set to ‘11’, the SOF pulse is also generated for the continuation SMD values: SMD-C[0,1,2,3] (0x61, 0x52, 0x9E or 0x2A).

5.11 Signal Quality Index

5.11.1 BACKGROUND

MLT-3 modulation is used for data transmission in 100BASE-TX and PAM5 modulation is used for data transmission in 1000BASE-T.

Logically, 100BASE-TX (MLT-3) and 1000BASE-T (PAM5) have signal values of {-1, 0, +1} and {-2, -1, 0, +1, +2}, respectively. These logic levels are mapped to slicer reference levels of {-128, 0, 128} for 100BASE-TX and {-128, -64, 0, 64, 128} for 1000BASE-T. The middle points (the compare thresholds) are {-64, 64} for 100BASE-TX and are {-96, -32, 32, 96} for 1000BASE-T.

Ideally, each receive data sample would be the maximum distance from the compare thresholds, with error values of 0. But because of noise and imperfection in real applications, the sampled data may be off from its ideal. The closer to the compare threshold, the worse the signal quality.

The slicer error is a measurement of how far the processed data is off from its ideal location. The largest instantaneous slicer error for 1000BASE-T is ±32. The largest instantaneous slicer error for 100BASE-TX is ±64.

A higher absolute slicer error means a degraded signal receiving condition.

5.11.2 NON OPEN ALLIANCE LOW PASS FILTERED ERROR

Note:	All registers references in this section are in Extended Page 1.

With this method, the slicer error is converted into an absolute value and then filtered by a programmable low pass filter. This is similar to taking the average of absolute slicer error over a long moving time window.

This mode is enabled by setting the sqi_enable bit in the Dynamic Channel Quality (DCQ) Configuration register.

For each data sample, the difference between the absolute slicer error (scaled by x2 (before squaring) for 1000BASE-T) and the current filtered value is added back into the current filtered value. The sqi_squ_mode_en bit in the DCQ Configuration register is used to square the (scaled) slicer error.

The sqi_kp field in the DCQ Configuration register sets the weighting of the add back as a divide by $2^{\wedge sqi_kp}$, effectively setting the filter bandwidth. As the sqi_kp value is increased, the weighing is decreased, and the mean slicer error value takes a longer time to settle to a stable value. Also, as the sqi_kp value is increased, there will be less variation in the mean slicer error value reported.

The filtered error value is saved every 1.0 ms (125,000 symbols).

In order to capture the current error value, the DCQ Read Capture bit in the DCQ Configuration register needs to be written as a high with the desired cable pair specified in the DCQ Channel Number field of the same register. The DCQ Read Capture bit immediately self-clears and the result is available in the Mean Slicer Error register.

A software based lookup table (derived empirically in lab conditions) may be used to report a Signal Quality Index (SQI) number.

5.11.3 OPEN ALLIANCE TC1/TC12 DCQ MEAN SQUARE ERROR

Note:	All registers references in this section are in Extended Page 1.

This section defines the implementation of section 6.1.1 of the TC1 and TC12 specifications. The PHY can provide detailed information of the dynamic signal quality by means of an MSE value. This mode is enabled by setting the sqi_enable bit in the DCQ Configuration register.

With this method, the slicer error is converted into a squared value and then filtered by a programmable low pass filter. This is similar to taking the average of absolute slicer error over a long moving time window.

For each data sample, the difference between the absolute slicer error (scaled by x2 (before squaring) for 1000BASE-T) and the current filtered value is added back into the current filtered value.

The sqi_squ_mode_en bit in the DCQ Configuration register must be set to choose square mode.

The sqi_kp field in the DCQ Configuration register sets the weighting of the add back as a divide by $2^{\wedge sqi_kp}$, effectively setting the filter bandwidth. As the sqi_kp value is increased, the weighing is decreased, and the mean slicer error value takes a longer time to settle to a stable value. Also, as the sqi_kp value is increased, there will be less variation in the mean slicer error value reported.

The scale611 field in the DCQ Configuration register is used to set a divide by factor (divide by $2^{\wedge scale611)}$ such that the Mean Squared Error (MSE) value is linearly scaled to the range of 0 to 511. If the divide by factor is too small, the MSE value is capped at a maximum of 511.

The filtered error value is saved every 1.0 ms (125,000 symbols).

In order to capture the MSE value, the DCQ Read Capture bit in the DCQ Configuration register needs to be written as a high with the desired cable pair specified in the DCQ Channel Number field of the same register. The DCQ Read Capture= bit will immediately self-clear and the result will be available in the DCQ Mean Square Error register.

In addition to the current MSE value the worst case MSE value since the last read of DCQ Mean Square Error register is stored in DCQ Mean Square Error Worst Case register.

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5.11.4 OPEN ALLIANCE TC1/TC12 DCQ SIGNAL QUALITY INDEX

Note: All registers references in this section are in Extended Page 1.

This section defines the implementation of section 6.1.2 of the TC1 and TC12 specifications. This mode builds upon the OPEN Alliance TC1/TC12 DCQ Mean Square Error method by mapping the MSE value onto a simple quality index. This mode is enabled by setting the sqi_enable bit, in the DCQ Configuration register.

Note: As in the OPEN Alliance TC1/TC12 DCQ Mean Square Error method, the sqi_squ_mode_en bit in the DCQ Configuration register must be set to choose square mode.

Note: As above in the OPEN Alliance TC1/TC12 DCQ Mean Square Error method, the scale611 field in the DCQ Configuration register is used to set the divide by factor (divide by $2^{\wedge scale611)}$ such that the MSE value is linearly scaled to the range of 0 to 511.

The MSE value is compared to the thresholds set in the DCQ SQI Table Registers to provide an SQI value between 0 (worst value) and 7 (best value) as follows:

TABLE 5-3: MSE TO SQI MAPPING

MSE Value		SQI Value
Greater Than	**Less Than or Equal To**	
—	SQI_TBL7.SQI_VALUE	7
SQI_TBL7.SQI_VALUE	SQI_TBL6.SQI_VALUE	6
SQI_TBL6.SQI_VALUE	SQI_TBL5.SQI_VALUE	5
SQI_TBL5.SQI_VALUE	SQI_TBL4.SQI_VALUE	4
SQI_TBL4.SQI_VALUE	SQI_TBL3.SQI_VALUE	3
SQI_TBL3.SQI_VALUE	SQI_TBL2.SQI_VALUE	2
SQI_TBL2.SQI_VALUE	SQI_TBL1.SQI_VALUE	1
SQI_TBL1.SQI_VALUE	—	0

In order to capture the SQI value, the DCQ Read Capture bit in the DCQ Configuration register needs to be written as a high with the desired cable pair specified in the DCQ Channel Number field of the same register. The DCQ Read Capture bit will immediately self-clear and the result will be available in the DCQ SQI register.

In addition to the current SQI, the worst case (lowest) SQI since the last read is available in the SQI Worst Case field.

The correlation between the SQI values stored in the DCQ SQI register and an according Signal to Noise Ratio (SNR) based on Additive White Gaussian (AWG) noise (bandwidth of 80 MHz @ 100 Mbps / 550 MHz @ 1000 Mbps) is shown in Table 5-4 and Table 5-5. The bit error rates to be expected in the case of white noise as interference signal is shown in the table as well for information purposes.

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A link loss only occurs if the SQI value is 0.

TABLE 5-4: 1000M SQI PERFORMANCE

SQI Value	Link State	Bit Error Rate (BER)
7	Up	$< 10^{-10}$ No frame drops
6	Up	
5	Up	
4	Up	$> 10^{-10}$ Frame drops may occur
3	Up	
2	Up	
1	Up	
0	Intermittent / Down	Heavy frame drops may occur

TABLE 5-5: 100M SQI PERFORMANCE

SQI Value	Link State	Bit Error Rate (BER)
7	Up	$< 10^{-10}$ No frame drops
6	Up	
5	Up	
4	Up	
3	Up	
2	Up	
1	Up	
0	Intermittent / Down	$> 10^{-10}$ Frame drops may occur

5.11.5 OPEN ALLIANCE TC1/TC12 DCQ PEAK MSE VALUE

Note: All registers references in this section are in Extended Page 1.

This section defines the implementation of section 6.1.3 of the TC1 and TC12 specifications. The peak MSE value is intended to identify transient disturbances, which are typically in the microsecond range. This mode is enabled by setting the sqi_enable bit, in the DCQ Configuration register.

With this method, the slicer error is converted into a squared value and then filtered by a programmable low pass filter. This is similar to taking the average of absolute slicer error over a moving time window.

For each data sample, the difference between the absolute slicer error (scaled by x2 (before squaring) for 1000BASE-T) and the current filtered value is added back into the current filtered value.

Note: The sqi_squ_mode_en bit in the DCQ Configuration register must be set to choose square mode.

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The sqi_kp3 field in the DCQ Configuration register sets the weighting of the add back as a divide by $2^{\wedge(sqi_kp3)}$, effectively setting the filter bandwidth. As the sqi_kp3 value is increased, the weighing is decreased, and the mean slicer error value takes a longer time to settle to a stable value.

Every 1.0 ms (125,000 symbols), the highest filtered value over that previous 1.0 ms period is saved.

The scale613 field in the DCQ Configuration register is used to set a divide by factor (divide by $2^{\wedge scale613+3)}$ such that the peak MSE value is linearly scaled to the range of 0 to 63. If the divided by factor is too small, the peak MSE value is capped at a maximum of 63.

In order to capture the peak MSE value, the DCQ Read Capture bit in the DCQ Configuration register needs to be written as a high with the desired cable pair specified in the DCQ Channel Number field of the same register. The DCQ Read Capture bit will immediately self-clear and the result will be available in the DCQ Peak MSE register.

In addition to the current peak MSE value, the worst case peak MSE value since the last read of DCQ Peak MSE register is stored in the same register.

5.12 Loopbacks

The device supports the following loopback operations to verify analog and/or digital paths:

- Digital (Near-End) Loopback
- Remote (Far-End) Loopback
- External Connector Loopback
- QSGMII Loopback

All loopbacks are enabled on an individual per-port basis.

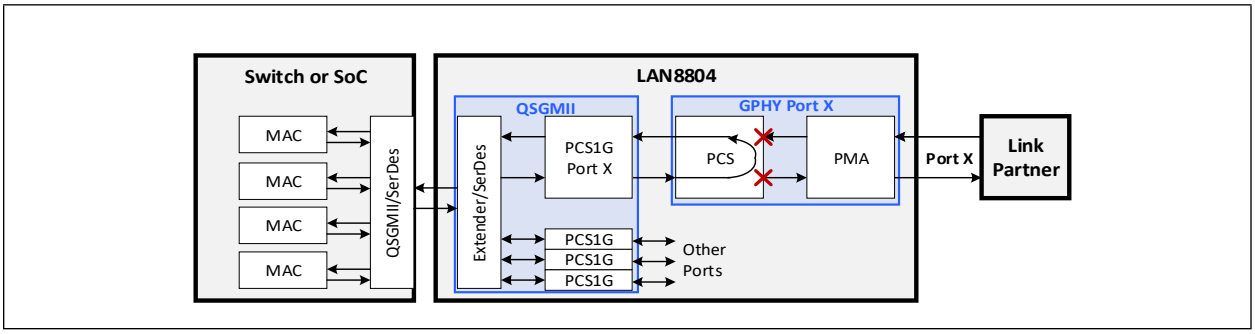
5.12.1 DIGITAL (NEAR-END) LOOPBACK

This loopback mode checks the QSGMII transmit and receive data paths between the device and the external MAC, and is supported for all three speeds (10/100/1000 Mbps) at full-duplex.

The loopback data path is shown in Figure 5-3.

1. QSGMII MAC transmits frames to the device.
2. Frames are wrapped around inside the device.
3. The device transmits frames back to QSGMII MAC.

FIGURE 5-3: DIGITAL (NEAR-END) LOOPBACK



5.12.2 REMOTE (FAR-END) LOOPBACK

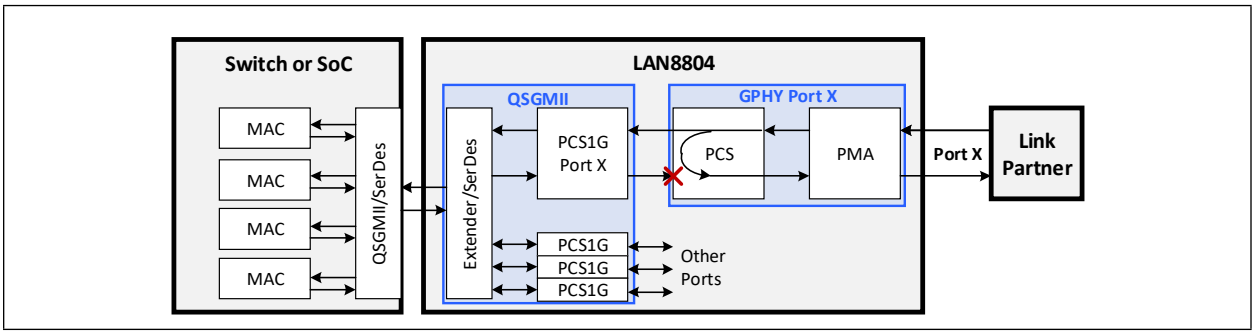
This loopback mode checks the line (differential pairs, transformer, RJ-45 connector, Ethernet cable) transmit and receive data paths between the device and its link partner, and is supported for 1000BASE-T full-duplex mode only.

The loopback data path is shown in Figure 5-4.

1. The Gigabit PHY link partner transmits frames to the device.
2. Frames are wrapped around inside the device.

3. The device transmits frames back to the Gigabit PHY link partner.

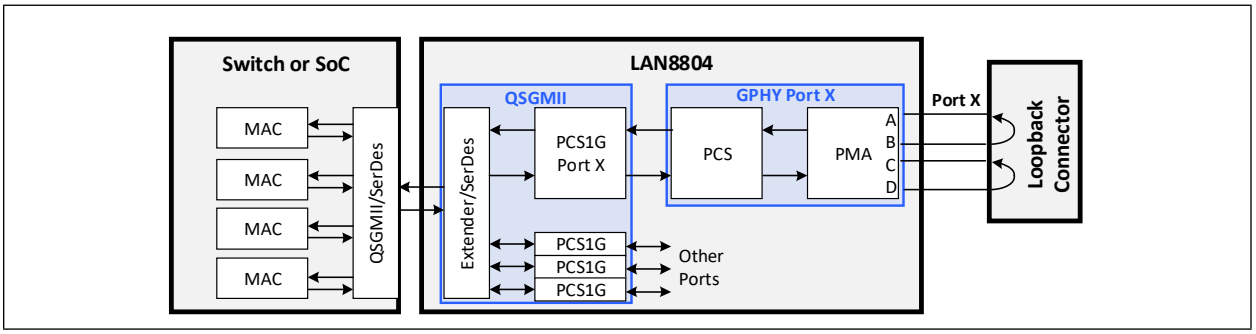
FIGURE 5-4: REMOTE (FAR-END) LOOPBACK



5.12.3 EXTERNAL CONNECTOR LOOPBACK

The external connector loopback testing feature allows the twisted pair interface to be looped back externally. This loopback tests the PHY digital and MAC connectivity. When using this feature, the PHY must be connected to a loopback connector or a loopback cable. Pair A must be connected to pair B, and pair C to pair D, as shown in Figure 5-5. The connector loopback feature functions at all available interface speeds.

FIGURE 5-5: EXTERNAL CONNECTOR LOOPBACK

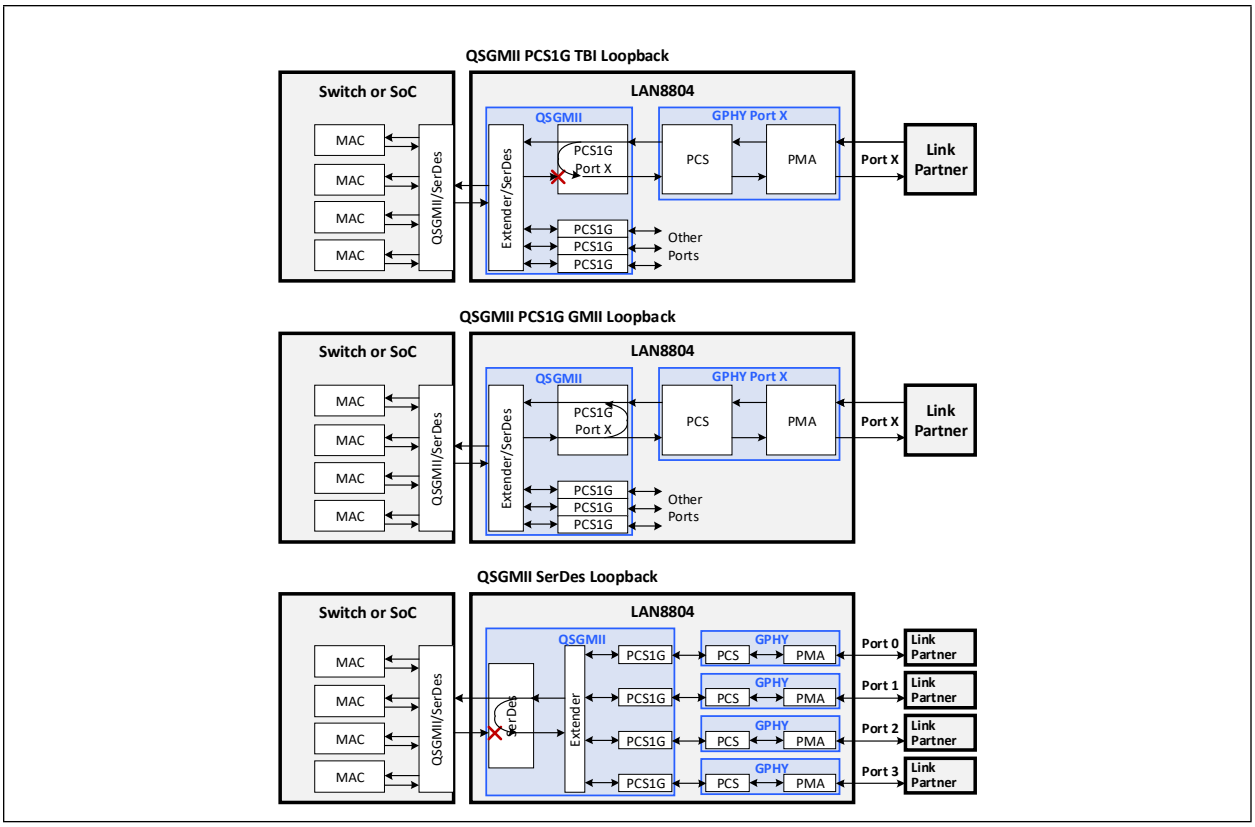


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5.12.4 QSGMII LOOPBACK

This QSGMII loopback testing feature calls various portions of the QSGMII block to be tested, as shown in Figure 5-5. When frames are looped in the QSGMII PCS1G, individual ports are looped, not the entire QSGMII. When frames are looped in the QSGMII SerDes, all four ports are looped.

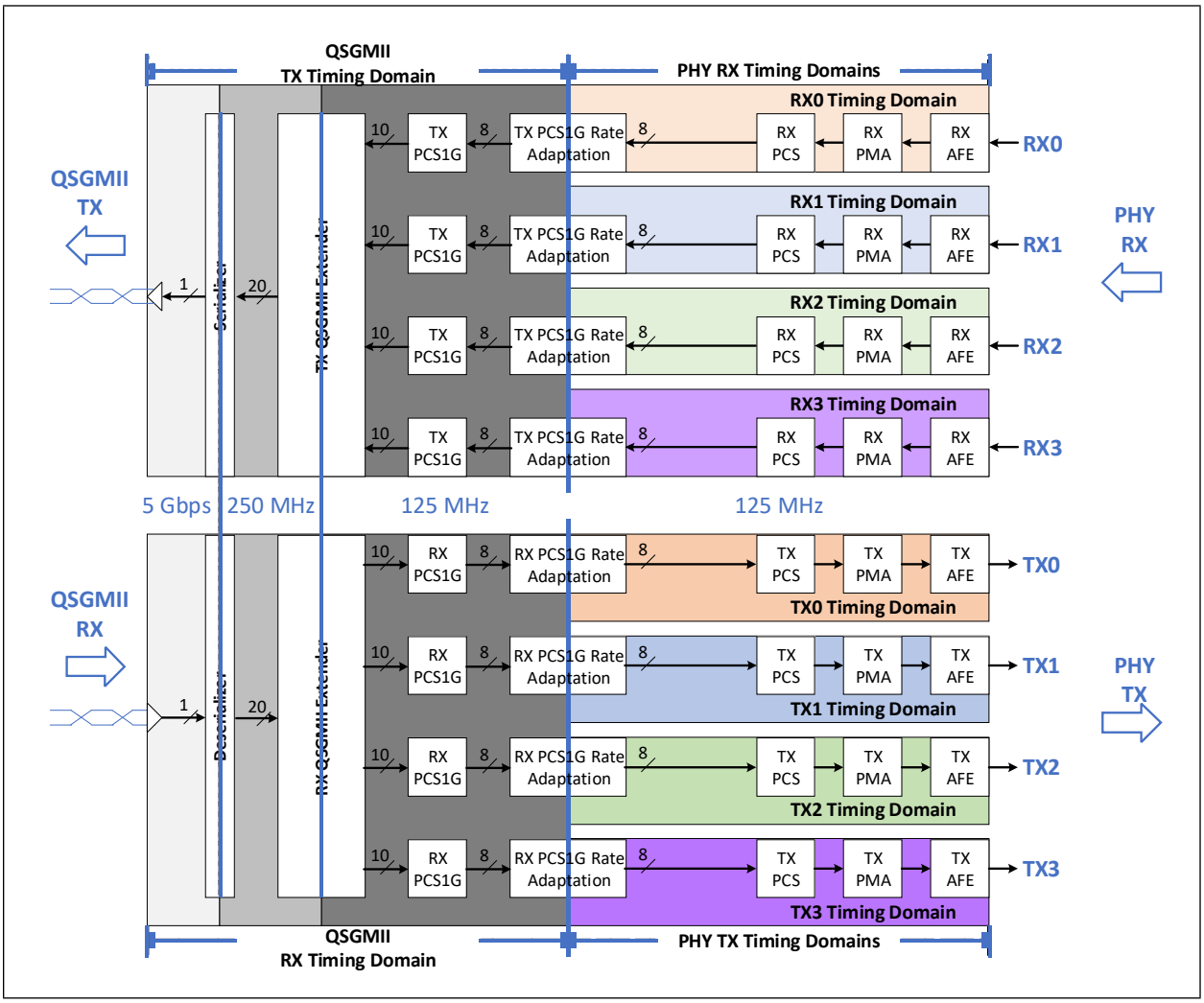
FIGURE 5-6: QSGMII LOOPBACK



5.13 QSGMII

The device provides a QSGMII interface that adheres to the QSGMII Specification Rev. 1.3 [4] (EDCS-540123). QSGMII is a serial chip-chip connection that connects the LAN8804 PHY ports with four MACs in the Switch or SoC. Figure 5-7 illustrates QSGMII operation, with the switch/SoC on the left and the LAN8804 on the right.

FIGURE 5-7: QSGMII SYSTEM DIAGRAM



Each device PHY connects to an SGMII “PCS1G” block (each is shown in Figure 5-7 as a separate TX PCS1G and RX PCS1G). The four SGMII TX PCS1G outputs are multiplexed together by the TX QSGMII Extender, which then swaps the Port 0 K28.5 symbol to K28.1 for Port 0 in the TX QSGMII Extender, before multiplexing the four ports together.

Each PCS1G instance includes a Jitter Test Pattern (JTP) Generator and Checker. The JTP Generator supports the following test patterns:

- High Frequency Test Pattern – repeated transmission of D21.5 code group
- Low Frequency Test Pattern – repeated transmission of K28.7 code group
- Mixed Frequency Test Pattern – repeated transmission of K28.5 code group
- Long Continuous Random Test Pattern – 1524 byte frames
- Short Continuous Random Test Pattern – 360 byte frames

The JTP Checker provides Checker Lock and Error Detected indications, as well as an error count.

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The RX QSGMII Extender uses the K28.1 symbol to locate Port 0, then swaps the K28.1 symbol back to the original K28.5, before sending the four demultiplexed streams to their RX PCS1G blocks.

Note: PHY TX and RX directions are relative to the Ethernet Media Interfaces. QSGMII TX and RX directions are relative to the QSGMII SerDes interface. So device frames received from the Ethernet Media Interfaces are processed in RX GPHY and in TX QSGMII blocks.

Note: If Energy Efficient Ethernet (EEE) is enabled, it is controlled using LPI symbols, which pass transparently through QSGMII.

Note: Coma mode has no effect on QSGMII functions.

QSGMII loopbacks are discussed in Section 5.12.4, "QSGMII Loopback".

5.14 MIIM (MDIO) Interface

The device supports the IEEE 802.3 MII management interface, also known as the Management Data Input/Output (MDIO) interface. This interface allows upper-layer devices to monitor and control the state of the device. An external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. More details about the MIIM interface can be found in Clause 22.2.4 of the IEEE 802.3 Specification [1].

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (**MDC**) and the data line (**MDIO**).
- A specific protocol that operates across the physical connection mentioned earlier, which allows an external controller to communicate with one or more devices. Each device is assigned a unique PHY address between 0h and 1Fh by the **PHYAD[4:0]** strapping pins. Refer to Section 3.3.3, "All PHYs Address (ALLPHYAD)" for additional information.
- A 32-register address space for direct access to IEEE-defined registers and vendor-specific registers, and for indirect access to MMD addresses and registers.

Table 5-6 shows the MII management frame format for the device.

TABLE 5-6: MII MANAGEMENT FRAME FORMAT

	Preamble	Start of Frame	Read/Write OP Code	PHY Address Bits[4:0]	REG Address Bits[4:0]	TA	Data Bits[15:0]	Idle
Read	32 1's	01	10	AAAAA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1's	01	01	AAAAA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

Note: This device may respond to Clause 45 accesses and so must not be mixed with Clause 45 devices on the same MDIO bus.

5.14.1 HIGH-SPEED MDIO OPERATION

The MDIO bus can operate at standard speeds up to 2.5 MHz, as well as higher speeds up to 25 MHz. Default register values enable standard MDIO operation using open-drain MDIO drivers, which is MDIO operation up to 2.5 MHz MDC frequency with daisy-chained PHYs on the MDIO bus. Due to open-drain drivers, an external 1 kΩ pull-up resistor is required.

Higher speed MDIO operation up to 25 MHz is supportable but requires reconfiguring the device to use push-pull MDIO drivers, and does not allow daisy-chaining PHYs on the MDIO bus. The reconfiguration process requires initially running the MDIO bus at 2.5 MHz using open-drain MDIO drivers and the external 1 kΩ pull-up resistor. The push-pull MDIO drivers allow operation up to 25 MHz with the 1 kΩ pull-up resistor.

5.14.2 ALL PHYS ADDRESS

Normally, the Ethernet PHYs are accessed at the PHY addresses set by the **PHYAD[4:0]** strapping pins.

PHY Address 0h is optionally supported as the broadcast PHY address, which allows for a single write command to simultaneously program an identical PHY register for two or more PHY devices (for example, using PHY Address 0h to set the Basic Control register to a value of 0x1940 to set bit[11] to a value of one to enable software power-down).

PHY Address 0 is enabled (in addition to the PHY address set by the **PHYAD[4:0]** strapping pins) when the All-PHYAD Enable bit in the Common Control register is set to '1'. The **ALLPHYAD** configuration strap can also be used to set the default of the All-PHYAD Enable bit.

5.14.3 MDIO OUTPUT DRIVE MODE

The **MDIO** output pin drive mode is controlled by the MDIO Buffer Type bit in the Output Control register. When set to a '0', the **MDIO** output is open-drain. When set to '1', the **MDIO** output is push-pull.

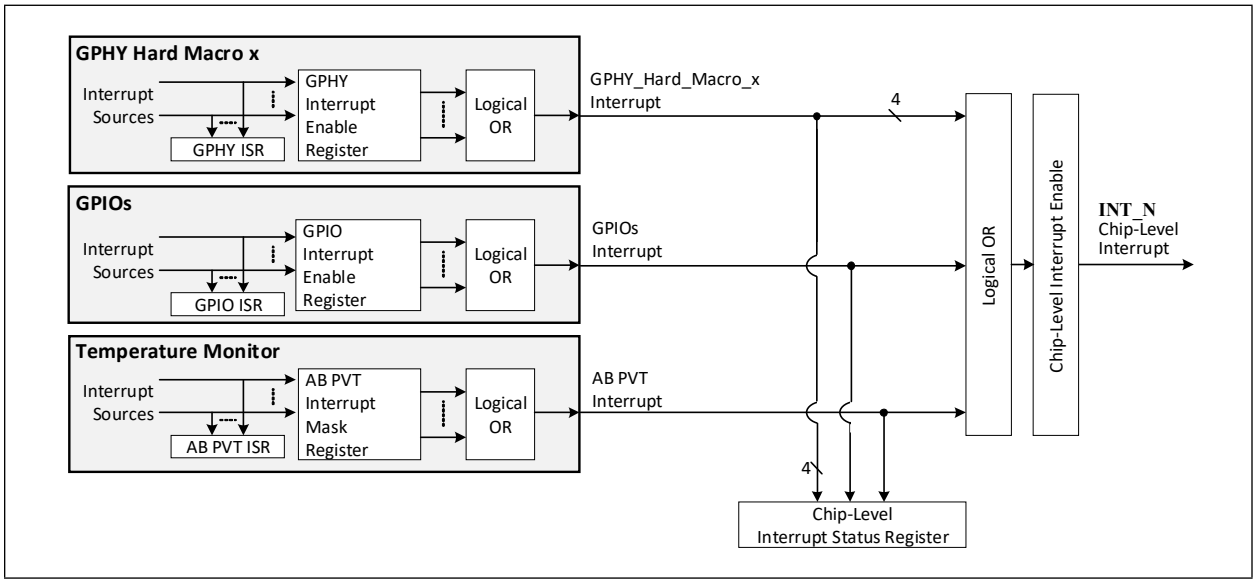
5.15 Interrupts

The **INT_N** pin is an optional interrupt signal that is used to inform the external controller that there has been a status update in the device. The Interrupt Enable register contains the interrupt control bits that enable and disable the conditions for asserting the **INT_N** signal. The Interrupt Status register contains the interrupt status bits that indicate which interrupt conditions have occurred. Most interrupt status bits are cleared upon reading. Some bits are read only and have a lower level register to indicate individual sources.

Note:	Bits in the Interrupt Status register are set by the interrupt events regardless of the value of the corresponding bits in the Interrupt Enable register.

The interrupt structure of the device is detailed in Figure 5-8.

FIGURE 5-8: INTERRUPT STRUCTURE



The **INT_N** buffer type is selectable between open-drain and push-pull and is configured by the INT Buffer Type field in the Output Control register. The default is open-drain.

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The Intr Polarity Invert bit in the Control register sets the interrupt level to active high or active low. The default is active low. If the buffer type is set to open-drain, the polarity is forced to be active low.

5.16 GPIOs

The General Purpose I/Os (GPIOs) consist of 24 programmable input/output pins that are shared with other pins. These pins are individually configurable via the GPIO registers.

GPIOs support the following functions:

- Software-readable GPIO. The GPIO is an input and its value can be directly read via the GPIO Data register. In addition, these GPIOs can also be configured to generate interrupts.
- Software-writable GPIO. The GPIO is an output and its value can be directly set via the GPIO Data register.
- GPIO Alternate Function. The GPIO pin is shared with some other function. Depending on the alternate function, the GPIO pin may be either an input or output. If the GPIO pin is an input, it can still be configured to perform any GPIO input function in addition to the alternate function.

For a pin to function as its GPIO, the GPIO must be enabled via the corresponding bit in the GPIO Enable Registers.

When configured as an input, via the GPIO Direction register (GPIO_DIR1 or GPIO_DIR2), the pin's pull-up is enabled. Each bit in the GPIO Data Registers reflects the current state of the corresponding GPIO input.

Note:	Extreme care must be taken on strap input pins that may be used for General Purpose Inputs. The General Purpose Inputs must be conditioned or otherwise disabled such that they do not drive incorrect strap input values during the strap loading time.

When configured as an output, the output buffer type is selected by the corresponding bit in the GPIO Buffer Type Registers. Push/pull and open-drain output buffers are supported for each GPIO.

- When functioning as an open-drain driver, the GPIO output pin is driven low when the corresponding bit in the GPIO Data Registers is cleared to '0' and is not driven when set to '1'.
- When functioning as a push/pull output, the GPIO output pin is driven low or high by the corresponding bit in the GPIO Data Registers.

When a GPIO is set to an output, the pin's pull-up is disabled, however the pin's input buffer remains enabled. A read of the GPIO Data Registers returns the state of the GPIO inputs (not the previous values written to these registers).

5.16.1 GPIO ALTERNATE FUNCTIONS

Many GPIOs have the ability to be used as an alternate function. Once enabled as a GPIO, the alternate function is selected by the bits in the GPIO Alternate Function Select Registers.

The alternate function buffer type is still selected via the GPIO Buffer Type Registers. If the alternate function is a Port LED and the GPIO Buffer Type is open-drain, the output buffer will automatically select between open-source and open-drain based on the applicable LED Polarity.

Alternate Functions input pins can be read by software via the GPIO Data register, can generate GPIO Interrupts. Table 5-7 describes the alternate function mappings. Alternate functions are each described fully in Section 3.0, "Pin Descriptions and Configuration".

TABLE 5-7: GPIO ALTERNATE FUNCTIONS

GPIO	Alternate Function	Configuration Strap	Comments
GPIO23	SOF3	—	—
GPIO22	—		
GPIO21	SOF1		

TABLE 5-7: GPIO ALTERNATE FUNCTIONS (CONTINUED)

GPIO	Alternate Function	Configuration Strap	Comments
GPIO20	PORT2LED2	PORT2_LED2_POL	To enable LED operation with either a pull-up or pull-down, LED Polarity takes on the inverted value of the configuration strap. Refer to Section 5.17, "LEDs" and Section 3.3.5, "LED Polarity (PORT[3:0]_LED[2:1]_POL)" for additional information.
GPIO19	PORT2LED1	PORT2_LED1_POL	
GPIO18	PORT1LED2	PORT1_LED2_POL	
GPIO17	PORT1LED1	PORT1_LED1_POL	
GPIO16	SOF2	PHYAD4	—
GPIO15	SOF0	PHYAD3	
GPIO14	PORT3LED2	PHYAD2/ PORT3_LED2_POL	To enable LED operation with either a pull-up or pull-down, LED Polarity takes on the inverted value of the configuration strap. Refer to Section 5.17, "LEDs" and Section 3.3.5, "LED Polarity (PORT[3:0]_LED[2:1]_POL)" for additional information.
GPIO13	PORT3LED1	PHYAD1/ PORT3_LED1_POL	
GPIO12	PORT0LED2	PHYAD0/ PORT0_LED2_POL	
GPIO11	PORT0LED1	LED_MODE/ PORT0_LED1_POL	
GPIO10	—	—	—
GPIO9	—		
GPIO8	—		
GPIO7	—		
GPIO6	—	MODE_SEL4	
GPIO5	—	MODE_SEL3	
GPIO4	—	MODE_SEL2	
GPIO3	—	MODE_SEL1	
GPIO2	—	—	
GPIO1	—	MODE_SEL0	
GPIO0	—	ALLPHYAD	

Note: The following must be considered when using GPIOs:

- Configuring a pin as a GPIO input automatically enables an internal pull-up.
- Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
- Configuring a pin as a GPIO output automatically disables the internal pull-up. Open-drain outputs may require an external pull-up depending on the application.

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5.16.2 GPIO INTERRUPTS

Each GPIO provides the ability to trigger a unique GPIO interrupt in the GPIO Interrupt Status Registers. Reading the GPIO Interrupt Status Registers provides the current status of all GPIO interrupts. Each interrupt is enabled by setting the corresponding bit in the GPIO Interrupt Enable Registers. The GPIO Controller aggregates the enabled interrupt values into an internal signal that is sent to the main interrupt logic and is reflected via the GPIO Interrupt bit in the Chip-level Interrupt Status register.

Bits in the GPIO Interrupt Status Registers are set by the interrupt events regardless of the value of the corresponding bits in the GPIO Interrupt Enable Registers.

Note:	Upon reset, GPIOs that were outputs may generate an active interrupt status as the system settles—typically when a low GPIO pin slowly rises due to the internal pull-up. The interrupt status bits within the GPIO Interrupt Status Registers must be cleared as part of the device initialization software routine.

Each GPIO interrupt polarity can be set individually via the GPIO Interrupt Polarity Registers. When the Interrupt Polarity bit is set to '1', a high logic level on the GPIO pin will set the corresponding interrupt bit in the GPIO Interrupt Status Registers. When the Interrupt Polarity bit is set to '0', a low logic level on the GPIO pin will set the corresponding interrupt bit in the GPIO Interrupt Status Registers.

5.16.3 GPIO TIMING

For GPIO timing information, refer to the following Section 6.6, "AC Specifications" sub-sections:

- GPIO Timing
- GPIO SOF Detection Timing

5.17 LEDs

The device provides eight programmable LEDs, two per port (**PORT[0:3]LED[1:2]**), which are configurable to support multiple LED modes. The LED mode is configured by the **LED_MODE** configuration strap as well as port-specific instances of the LED Control Register 1 and 2. All eight LEDs are configured with identical behavior via the **LED_MODE** configuration strap. Port-specific LED configuration can be accomplished via the LED Control Register 1 and 2. The supported LED modes are:

- Individual-LED Mode (LED Control Register 1, bit[6] (KSZ0931 LED mode) = '1', **LED_MODE** pulled-up)
- Tri-color-LED Mode (LED Control Register 1, bit[6] (KSZ0931 LED mode) = '1', **LED_MODE** pulled-down)
- Enhanced LED Mode (LED Control Register 1, bit[6] (KSZ0931 LED mode) = '0', **LED_MODE** unused)

To use LEDs, they must be enabled as GPIOs and GPIO Alternate Functions. The GPIOs must be configured as Outputs, and the proper output driver type selected (open-drain or push-pull). If open-drain type is selected, the output driver will automatically choose between open-source and open-drain based on LED polarity.

The **PORT[3:0]_LED[2:1]_POL** configuration straps set the default polarity of the LED pins. Refer to Section 3.3.5, "LED Polarity (PORT[3:0]_LED[2:1]_POL)" for additional LED polarity information. Refer to Section 3.3.4, "LED Mode Select (LED_MODE)" for additional **LED_MODE** information.

Note:	Coma mode disables all LED functions. When the Coma mode input transitions from low to high, LED functions begin normal operation. Refer to Section 5.18, "Coma Mode" for additional information.

5.17.1 INDIVIDUAL-LED MODE

In Individual-LED mode, the **PORT*x*LED2** pin indicates the link status while the **PORT*x*LED1** pin indicates the activity status, as shown in Table 5-8.

Note:	The LEDs are forced off when any of the following occurs: • The Isolate (PHY_ISO) bit in the Basic Control register is set. • The Power Down bit in the Basic Control register is set. • Coma mode is asserted via the **COMA_MODE** pin.

TABLE 5-8: INDIVIDUAL-LED MODE OPERATION

PORT*x*LED2	PORT*x*LED1	Definition
Inactive	Inactive	No link
Active	Inactive	Link any speed, no activity
Active	Blinking	Link any speed, TX or RX activity
Other States		N/A

5.17.2 TRI-COLOR-LED MODE

In Tri-color-LED mode, the link and activity status are indicated by the **PORT*x*LED2** pin for 1000BASE-T; by the **PORT*x*-LED1** pin for 100BASE-TX; and by both **PORT*x*LED2** and **PORT*x*LED1** pins, working in conjunction, for 10BASE-T. This is summarized in Table 5-9.

Note: The LEDs are forced off when any of the following occurs:

- The Isolate (PHY_ISO) bit in the Basic Control register is set.
- The Power Down bit in the Basic Control register is set.
- Coma mode is asserted via the **COMA_MODE** pin.

TABLE 5-9: TRI-COLOR-LED MODE OPERATION

PORT*x*LED2	PORT*x*LED1	Definition
Inactive	Inactive	No link
Inactive	Active	100 Mbps link, no activity
Inactive	Blinking	100 Mbps link, TX or RX activity
Active	Inactive	1000 Mbps link, no activity
Blinking	Inactive	1000 Mbps link, TX or RX activity
Active	Active	10 Mbps link, no activity
Blinking	Blinking	10 Mbps link, TX or RX activity
Other States		N/A

5.17.3 ENHANCED LED MODE

Enhanced mode is enabled when the KSZ9031 LED mode bit in the corresponding port's LED Control Register 1 is cleared. In Enhanced LED mode, each LED can be configured to display different status information that can be selected by setting the corresponding LED Configuration field of the port's LED Control Register 2. The modes are detailed in Table 5-10. The blink/pulse-stretch and other LED setting can be configured via the LED Behavior register.

Note: The LEDs are forced off when any of the following occurs:

- The Isolate (PHY_ISO) bit in the Basic Control register is set.
- The Power Down bit in the Basic Control register is set.
- Coma mode is asserted via the **COMA_MODE** pin.

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TABLE 5-10: EXTENDED MODE OPERATION

Mode	PORT*x*LED*y*	Definition
Enhanced Mode 0 (Link/Activity)	Inactive	No link
	Active	Link any speed, no activity any speed
	Blinking	Link any speed, activity any speed
Enhanced Mode 1 (Link1000/Activity)	Inactive	No 1000 Mbps link
	Active	1000 Mbps link, no 1000 Mbps activity
	Blinking	1000 Mbps link, 1000 Mbps activity
Enhanced Mode 2 (Link100/Activity)	Inactive	No 100 Mbps link
	Active	100 Mbps link, no 100 Mbps activity
	Blinking	100 Mbps link, 100 Mbps activity
Enhanced Mode 3 (Link10/Activity)	Inactive	No 10 Mbps link
	Active	10 Mbps link, no 10 Mbps activity
	Blinking	10 Mbps link, 10 Mbps activity
Enhanced Mode 4 (Link100/1000/Activity)	Inactive	No 100/1000 Mbps link
	Active	100/1000 Mbps link, no 100/1000 Mbps activity
	Blinking	100/1000 Mbps link, 100/1000 Mbps activity
Enhanced Mode 5 (Link10/1000/Activity)	Inactive	No 10/1000 Mbps link
	Active	10/1000 Mbps link, no 10/1000 Mbps activity
	Blinking	10/1000 Mbps link, 10/1000 Mbps activity
Enhanced Mode 6 (Link10/100/Activity)	Inactive	No 10/100 Mbps link
	Active	10/100 Mbps link, no 10/100 Mbps activity
	Blinking	10/100 Mbps link, 10/100 Mbps activity
Enhanced Mode 7	N/A	Reserved
Enhanced Mode 8 (Duplex/Collision)	Inactive	Half-Duplex link or no link
	Active	Full-Duplex link
	Blinking	Half-Duplex link, collisions detected
Enhanced Mode 9 (Collision)	Inactive	No collisions detected
	Active	N/A
	Blinking	Collisions detected
Enhanced Mode 10 (Activity)	Inactive	No activity
	Active	N/A
	Blinking	Activity

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TABLE 5-10: EXTENDED MODE OPERATION (CONTINUED)

Mode	PORT*x*LED*y*	Definition
Enhanced Mode 11	N/A	Reserved
Enhanced Mode 12 (Parallel Detect Fault)	Inactive	No parallel detect fault
	Active	Parallel detect fault
	Blinking	N/A
Enhanced Mode 13	N/A	Reserved
Enhanced Mode 14 (Force LED Off)	Inactive	LED off
	Active	N/A
	Blinking	N/A
Enhanced Mode 15 (Force LED On)	Inactive	N/A
	Active	LED on
	Blinking	N/A

5.18 Coma Mode

Coma mode is designed to hold the PHY in a suspended state until system initialization is complete. When enabled by driving the **COMA_MODE** pin high, all the errors, alarms, link up/down notifications, etc. are suppressed until **COMA_MODE** is driven low. This is useful in designs with multiple PHYs, as it allows all errors to be suppressed until the entire board is configured. Coma mode operates as per Table 5-11.

TABLE 5-11: COMA MODE OPERATION

Chip Function	Coma Mode Active
Gigabit PHY Hard Macros	Gigabit PHYs held in disabled state (except configuration registers). No data is sent to the line or MAC, no recovered clock, no interrupt/error/ etc. indications given to the system.
LEDs	LEDs inactive
Interrupt	Interrupts inactive
QSGMII PCS1G Block	No affect
QSGMII Extender	No affect
SerDes	No affect
System PLL	No affect
MDIO Functions	No affect

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5.19 Power Management

The device incorporates a number of power-management modes and features that provide methods to consume less energy. These are discussed in the following sections.

5.19.1 SMART POWER SAVING

For shorter cable lengths (< ~70 meters) the SNR is sufficiently high to allow the reduction of ADC resolution as well as DSP taps. Based on the detected cable length, the device automatically reduces power consumption by approximately 20 mW.

5.19.2 ENERGY-DETECT POWER-DOWN MODE

The device supports an Energy-Detect Power-Down (EDPD) mode to save power when there is no link partner sending signals.

In EDPD mode, the device shuts down all transceiver blocks, except for the transmitter and energy detect circuits. Power can be reduced further by extending the time interval between the transmissions of link pulses to check for the presence of a link partner. The periodic transmission of link pulses is needed to ensure the device and its link partner, when operating in the same low-power state and with Auto-MDI/MDI-X disabled, can wake up when the cable is connected between them.

By default, EDPD mode is disabled after power-up. EDPD is enabled by setting the p_edpd_en bit in the EDPD Control register within the MMD address space.

EDPD operation may be adjusted via the p_edpd_mask_timer[1:0], p_edpd_timer[1:0], and p_EDPD_random_dis fields in the EDPD Control register within the MMD address space.

The energy detection change status can be read from the Interrupt Status register. The current energy detection status can be read from the EDPD low power bit in the Analog Control Register 8.

While the p_edpd_en bit is set, the cable link status will be down, and the energy detection normally monitors pairs A and B for energy. If the link speed is forced to 1000 Mbps (by disabling auto-negotiation and setting the speed manually), the energy detection monitors all four pairs. For cable diagnostic purposes, individual wire pairs may be monitored by forcing the link speed to 1000 Mbps and selecting the wire pair using the EDPD Wire Pair Selection bits in the Analog Control Register 8.

The device's PLL is normally enabled during EDPD. It can be set to be disabled during EDPD by setting the DGT_edpd_pll_dis bit in MMD31 Register 19.

Normally, previous register setting are maintained when EDPD mode is cleared. With the PLL disabled, a device reset occurs following the removal of EDPD (or if the DGT_edpd_pll_dis bit is cleared during EDPD), in which case register settings will return to their defaults.

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5.19.3 SOFTWARE POWER-DOWN MODE

The device supports a Software Power-Down (SPD) mode. This mode is used to power down the device when it is not in use after power-up. SPD mode is enabled by writing a one to the Power Down bit in the Basic Control register. The device may also be placed into software power-down by default by setting the **MODE_SEL[4:0]** configuration straps to '0100x'. The device exits the SPD state after a zero is written to the Power Down bit.

In the SPD state, the device disables most internal functions. During SPD, the crystal oscillator and PLL are enabled and the internal (125 MHz and 250 MHz) clocks are gated. The standard registers (0 through 31) and the MII Management Interface operate using the crystal clock.

Previous register settings are maintained during and following the removal of SPD.

APPLICATION NOTE: The internal (125 MHz and 250 MHz) clock gating maybe overridden by setting the spd_clock_gate_override bit in the Digital Debug Control 2 register at the cost of increased power.

The following remain operational during SPD:

- MII Management Interface
  - Only access to the standard registers (0 through 31) is supported.
  - Access to MMD address spaces other than MMD Address Space 1 is possible if the spd_clock_gate_override bit is set.
  - Access to MMD Address Space 1 is not possible.
- Voltage Regulator Controller (LDO)
  - The LDO has been defeatured and **LDO_O** should be left disconnected. Microchip recommends disabling the LDO output by setting the active low LDO enable bit in the Analog Control Register 11. An external source of 1.21V is required for operation.
- PLL
  - Normally the PLL is enabled during SPD. It may be disabled by setting the spd_pll_disable bit described below.
- Crystal Oscillator
  - Normally the Crystal Oscillator is enabled during SPD. It may be disabled by setting the enXTALb bit described below.
- Bandgap
  - This is always enabled.
- Internal Slow Oscillator
  - This is always enabled.

The following are normally disabled during SPD:

- ADC/PGA/TX/common bias circuits
- DLL
- TX and RX clocks
  - If the above mentioned spd_clock_gate_override bit is set, TX and RX clocks would be enabled. They may alternately be stopped by setting the Isolate (PHY_ISO) bit in the Basic Control register.

5.19.3.1 SPD Extra Power Savings

To achieve a lower power usage, the PLL may be disabled during SPD mode by setting the spd_pll_disable bit in the Digital Debug Control 2 register prior to entering SPD. The device may also be placed into software power-down with the PLL disabled by default by setting the **MODE_SEL[4:0]** configuration straps to '01001'.

With the PLL disabled, a device reset occurs following the removal of SPD (or if the spd_pll_disable bit is cleared during SPD). Register settings will return to their defaults, determined by the Operation Mode Strap Override Low register and the Operation Mode Strap Override High register.

APPLICATION NOTE: If either the spd_pll_dis_mode or spd_pll_en_mode bits in the Operation Mode Strap Override Low register are set, the device will return to SPD mode, potentially with the PLL disabled. In order to avoid this logical loop, software must clear the spd_pll_dis_mode and spd_pll_en_mode bits before exiting SPD.

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To further reduce power usage, the crystal oscillator maybe disabled by setting the enXTALb bit in the Analog Control Register 1 after setting the spd_pll_disable bit and entering SPD.

Since the MII Management Interface operates using the crystal clock, once this bit is set, the device will become inaccessible. A pin reset or power cycle is required to resume operation.

5.20 PLL/Clocks and Resets

The device provides the following PLLs:

- **System PLL:** Generates the internal system clocks and clocks required for the internal PHYs. See Section 5.20.1, "System Clocks" for additional information.
- **QSGMII SerDes MPLL:** Generates the clocks needed by the SerDes. See Section 5.20.2, "QSGMII SerDes Clock" for additional information.

Note:	Coma mode has no effect on these functions. Refer to Section 5.18, "Coma Mode" for additional information.

The reference clock selection of the System PLL and QSGMII SerDes MPLL are controlled via the **REF_CLK_SEL[1:0]** pins. Refer to Table 3-5 for detailed **REF_CLK_SEL[1:0]** setting information.

5.20.1 SYSTEM CLOCKS

System clocks are generated by the System PLL and are used for many common (not port-specific) functions such as QSGMII TX and configuration registers. These clocks are also selectable by each PHY port for use as PHY TX timing.

The System PLL generates the following clocks:

- 250 MHz system clock
- 25 MHz system clock

The System PLL can use any of the following as its input reference clock:

- 25 MHz Crystal
- 25 MHz system single-ended reference clock input
- 125 MHz system differential clock inputs

5.20.2 QSGMII SERDES CLOCK

The 250 MHz QSGMII SerDes clock is generated by the SerDes MPLL.

The QSGMII SerDes MPLL can use any of these as its input reference clock:

- 25 MHz system clock (from crystal or single-ended external clock input)
- 125 MHz system differential clock inputs

5.20.3 RESETS

The device supports the following software resets from configuration registers:

- Chip hard and soft resets (all logic and macros in the chip)
  - Chip soft reset (EP4.9) does not reset the Gigabit PHYs. If needed, the GPHY Hard Macro soft reset must be used for this.
  - GPHY resistor calibration is also run based on the chip hard reset.
- QSGMII hard and soft resets (QSGMII SerDes, extender, and per-port PCS1Gs)
- QSGMII SerDes transmitter and receiver resets
- Port hard and soft resets (all port-specific logic and macros in each port)
  - Neither port hard reset (EP5.80) nor soft reset (EP5.81) will reset the GPHY. If needed, the GPHY Macro hard or soft reset must be used for this.
- Gigabit PHY hard macro hard and soft resets (per port)

The device also provides a **RESET_N** input pin. This pin must adhere to the timing requirements detailed in Section 6.6.2, "Power Sequence Timing" and Section 6.6.3, "Reset Pin Configuration Strap Timing". Release from reset is based on the **RESET_N** input pin transitioning from low to high.

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5.20.4 POWER ON READY (POR) WITH OVER/UNDER VOLTAGE PROTECTION

POR monitors three voltages (Refer to Table 6-13 for the exact specification):

- +1.1V Analog Power Supply (on **VDDAL_*x***) set for ~0.8V (typical) - it is assumed that **VDDCORE** and **VDDAL_*x*** are externally connected, therefore VDD is indirectly monitored.
- +2.5/3.3V Analog Power Supply (on **VDDAH_*x***) set for ~2.1V (typical)
- Variable I/O Power Supply (on **VDDIO**) set for ~1.5V (typical)

The POR circuits have a “dead zone” between bottom range of valid operational voltage and where POR trips (e.g., -15%/20%). The Over/Under Voltage Protection enables tightening this range to just under the bottom of the supply range.

5.21 JTAG

An IEEE 1149.1 compliant TAP Controller supports boundary scan and various test modes.

The device includes an integrated JTAG boundary-scan test port for board-level testing. The interface consists of four pins (**TDO**, **TDI**, **TCK** and **TMS**) and includes a state machine, data register array and an instruction register. The JTAG pins are described in Table 3-6. The JTAG interface conforms to the IEEE Standard 1149.1 - 2001 *Standard Test Access Port (TAP) and Boundary-Scan Architecture*.

All input and output data is synchronous to the **TCK** test clock input. TAP input signals **TMS** and **TDI** are clocked into the test logic on the rising edge of **TCK**, while the output signal **TDO** is clocked on the falling edge.

JTAG pins are multiplexed with the GPIO pins. The JTAG functionality is selected when the **TESTMODE** pin is asserted.

The implemented JTAG instructions and their OP Codes are shown in Table 5-12. JTAG timing information is provided in Section 6.6.6, "JTAG Timing".

TABLE 5-12: JTAG OP CODES

INSTRUCTION	OP CODE
CLAMP	4’b0000
EXTEST	4’b0001
(RESERVED)	4’b0010
(RESERVED)	4’b0011
INTEST	4’b0100
SAMPLE_PRELOAD	4’b0101
HIGHZ	4’b0110
HOST-IJTAG ACCESS	4’b0111
ID CODE	4’b1000
BYPASS	4’b1001 to 4’b1111

Note: The JTAG device ID is 00341445h.

Note: All digital I/O pins support IEEE 1149.1 operation. Analog pins do not support IEEE 1149.1 operation.

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6.0 OPERATIONAL CHARACTERISTICS

6.1 Absolute Maximum Ratings*

Supply Voltage (**VDDAL_*x***, **VDDTXL_SERDES**, **VDDCORE**) (Note 6-1) ..... -0.5V to +1.27V

Supply Voltage (**VDDAH**, **VDDAH_*x***, **VDD33REF**, **VDDIO**, **VDDIO_1**) (Note 6-1) ..... -0.5V to +3.63V

Input Voltage (all inputs) ..... -0.5V to +3.63V

Output Voltage (all outputs) ..... -0.5V to +3.63V

Storage Temperature (T_S) ..... -55°C to +150°C

Lead Temperature (soldering, 10s) ..... +260°C

Maximum Junction Temperature (T_J) ..... +125°C

HBM ESD Performance ..... +/- 4kV

Note 6-1 When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

*Stresses exceeding those listed in this section could cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at any condition exceeding those indicated in Section 6.2, "Operating Conditions**", Section 6.5, "DC Specifications", or any other applicable section of this specification is not implied.

6.2 Operating Conditions**

Supply Voltage (**VDDAL_*x***, **VDDTXL_SERDES**, **VDDCORE**) ..... (-5%/+5%) +1.15V to +1.27V

Supply Voltage (**VDDAH**, **VDDAH_*x***, **VDD33REF** @ 3.3V) ..... (-5%/+5%) +3.135V to +3.465V

Supply Voltage (**VDDAH**, **VDDAH_*x***, **VDD33REF** @ 2.5V) ..... (-5%/+5%) +2.375V to +2.625V

Supply Voltage (**VDDIO**, **VDDIO_1** @ 3.3V) ..... (-5%/+5%) +3.135V to +3.465V

Supply Voltage (**VDDIO**, **VDDIO_1** @ 2.5V) ..... (-5%/+5%) +2.375V to +2.625V

Supply Voltage (**VDDIO**, **VDDIO_1** @ 1.8V) ..... (-5%/+5%) +1.71V to +1.89V

Input Voltage (all inputs) ..... -0.3V to +3.63V

Output Voltage (all outputs) ..... -0.3V to +3.63V

Ambient Operating Temperature in Still Air (T_A) ..... Note 6-2

Note 6-2 0°C to +85°C for commercial version, -40°C to +85°C for industrial version.

**Proper operation of the device is guaranteed only within the ranges specified in this section.

6.3 Power Consumption

This section details the power consumption of the device as measured during various modes of operation at various operating voltages. Power dissipation is impacted by temperature, supply voltage and external source/sink requirements. All minimum measurements were taken at +25°C unless otherwise noted. All worst-case measurements were taken at +5% power supply and +125°C junction temperature.

Power consumption data is split into the following tables:

- Minimum Four Port Operation
  - Minimum Four Port (1.16V, 3.3V, 3.3V) Power Consumption
  - Minimum Four Port (1.16V, 2.5V, 2.5V) Power Consumption
  - Minimum Four Port (1.16V, 2.5V, 1.8V) Power Consumption
- Worst-Case Four Port Operation
  - Worst-Case Four Port (1.27V, 3.465V, 3.465V) Power Consumption
  - Worst-Case Four Port (1.27V, 2.625V, 2.625V) Power Consumption
  - Worst-Case Four Port (1.27V, 2.625V, 1.89V) Power Consumption

Note 6-3 1.21V Total includes: **VDDCORE**, **VDDAL_PLL**, **VDDAL_SERDES**, **VDDTXL_SERDES**, **VDDAL_CK125**

Note 6-4 VDD_{AH} Total includes: **VDDAH**, **VDDAH_SERDES**, **VDDAH_PLL_PTP**, **VDDAH_ABPVT**, **VDD33REF**, **VDDAH_P*x***

Note 6-5 VDD_{IO} Total includes: **VDDIO**, **VDDIO_1**

6.3.1 MINIMUM FOUR PORT OPERATION

All measurements were taken at +25°C unless otherwise noted.

TABLE 6-1: MINIMUM FOUR PORT (1.16V, 3.3V, 3.3V) POWER CONSUMPTION

Device Conditions	1.16V Total (mA) (Note 6-3)	3.3V VDD_{AH} Total (mA) (Note 6-4)	3.3V VDD_{IO} Total (mA) (Note 6-5)	Total Device Power (mW)
4 ports + QSGMII, 1000BASE-T Master link-up, No traffic	737	520	8.3	2597
4 ports + QSGMII, 1000BASE-T Slave link-up, no traffic	738	520	8.4	2600
4 ports + QSGMII, 100BASE-TX link-up, no traffic	251	267	11.8	1211
4 ports + QSGMII, 10BASE-T link-up, no traffic	111	239	19.1	979
4 ports + QSGMII, 10BASE-Te link-up, no traffic	106	239	19.1	973
4 ports + QSGMII, 1000BASE-T Master full-duplex, 100% utilization	765	519	5.1	2616
4 ports + QSGMII, 1000BASE-T Slave full-duplex, 100% utilization	765	519	4.9	2617
4 ports + QSGMII, 100BASE-TX full-duplex, 100% utilization	251	276	6.7	1222
4 ports + QSGMII, 10BASE-T full-duplex, 100% utilization	106	268	10.6	1042

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TABLE 6-1: MINIMUM FOUR PORT (1.16V, 3.3V, 3.3V) POWER CONSUMPTION (CONTINUED)

Device Conditions	1.16V Total (mA) (Note 6-3)	3.3V VDD_{AH} Total (mA) (Note 6-4)	3.3V VDD_{IO} Total (mA) (Note 6-5)	Total Device Power (mW)
4 ports + QSGMII, 10BASE-Te full-duplex, 100% utilization	106	261	10.5	1019
4 ports + QSGMII, 1000BASE-T Master, EEE Sleep state	213	396	8.1	1579
4 ports + QSGMII, 1000BASE-T Slave, EEE Sleep state	213	396	8.1	1578
4 ports + QSGMII, 100BASE-TX, EEE Sleep state	138	237	11.7	979
4 ports + QSGMII, Energy Detect Power Down mode, QSGMII up	90	31	0.7	207
4 ports + QSGMII, Software Power Down mode, QSGMII up	77	26	0.7	177
4 ports + QSGMII, Software Power Down mode, QSGMII down	24	11	0.7	66
4 ports + QSGMII, hardware reset	15	15	0.5	68

TABLE 6-2: MINIMUM FOUR PORT (1.16V, 2.5V, 2.5V) POWER CONSUMPTION

Device Conditions	1.16V Total (mA) (Note 6-3)	2.5V VDD_{AH} Total (mA) (Note 6-4)	2.5V VDD_{IO} Total (mA) (Note 6-5)	Total Device Power (mW)
4 ports + QSGMII, 1000BASE-T Master link-up, no traffic	750	475	4.0	2067
4 ports + QSGMII, 1000BASE-T Slave link-up, No traffic	749	475	4.1	2067
4 ports + QSGMII, 100BASE-TX link-up, no traffic	254	228	5.3	878
4 ports + QSGMII, 10BASE-T link-up, no traffic	109	186	8.6	613
4 ports + QSGMII, 10BASE-Te link-up, no traffic	108	186	8.5	610
4 ports + QSGMII, 1000BASE-T Master full-duplex, 100% utilization	776	475	2.6	2093
4 ports + QSGMII, 1000BASE-T Slave full-duplex, 100% utilization	777	475	2.7	2094
4 ports + QSGMII, 100BASE-TX full-duplex, 100% utilization	252	228	3.0	870

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TABLE 6-2: MINIMUM FOUR PORT (1.16V, 2.5V, 2.5V) POWER CONSUMPTION (CONTINUED)

Device Conditions	1.16V Total (mA) (Note 6-3)	2.5V VDD_{AH} Total (mA) (Note 6-4)	2.5V VDD_{IO} Total (mA) (Note 6-5)	Total Device Power (mW)
4 ports + QSGMII, 10BASE-T full-duplex, 100% utilization	108	229	4.8	709
4 ports + QSGMII, 10BASE-Te full-duplex, 100% utilization	108	216	4.8	675
4 ports + QSGMII, 1000BASE-T Master, EEE Sleep state	217	357	3.8	1154
4 ports + QSGMII, 1000BASE-T Slave, EEE Sleep state	217	357	3.8	1153
4 ports + QSGMII, 100BASE-TX, EEE Sleep state	140	193	5.3	656
4 ports + QSGMII, Energy Detect Power Down mode, QSGMII up	90	32	0.5	186
4 ports + QSGMII, Software Power Down mode, QSGMII up	80	24	0.3	153
4 ports + QSGMII, Software Power Down mode, QSGMII down	27	10	0.3	57
4 ports + QSGMII, hardware reset	15	17	0.3	60

TABLE 6-3: MINIMUM FOUR PORT (1.16V, 2.5V, 1.8V) POWER CONSUMPTION

Device Conditions	1.16V Total (mA) (Note 6-3)	2.5V VDD_{AH} Total (mA) (Note 6-4)	1.8V VDD_{IO} Total (mA) (Note 6-5)	Total Device Power (mW)
4 ports + QSGMII, 1000BASE-T Master link-up, No traffic	735	467	0.3	2019
4 ports + QSGMII, 1000BASE-T Slave link-up, no traffic	736	466	0.3	2019
4 ports + QSGMII, 100BASE-TX link-up, no traffic	249	224	0.5	849
4 ports + QSGMII, 10BASE-T link-up, no traffic	106	184	0.7	582
4 ports + QSGMII, 10BASE-Te link-up, no traffic	107	183	0.6	582
4 ports + QSGMII, 1000BASE-T Master full-duplex, 100% utilization	762	466	0.4	2048
4 ports + QSGMII, 1000BASE-T Slave full-duplex, 100% utilization	763	466	0.4	2049

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TABLE 6-3: MINIMUM FOUR PORT (1.16V, 2.5V, 1.8V) POWER CONSUMPTION (CONTINUED)

Device Conditions	1.16V Total (mA) (Note 6-3)	2.5V VDD_{AH} Total (mA) (Note 6-4)	1.8V VDD_{IO} Total (mA) (Note 6-5)	Total Device Power (mW)
4 ports + QSGMII, 100BASE-TX full-duplex, 100% utilization	248	224	0.4	847
4 ports + QSGMII, 10BASE-T full-duplex, 100% utilization	105	227	0.5	689
4 ports + QSGMII, 10BASE-Te full-duplex, 100% utilization	106	213	0.4	656
4 ports + QSGMII, 1000BASE-T Master, EEE Sleep state	212	352	0.4	1125
4 ports + QSGMII, 1000BASE-T Slave, EEE Sleep state	212	352	0.4	1125
4 ports + QSGMII, 100BASE-TX, EEE Sleep state	138	189	0.4	634
4 ports + QSGMII, Energy Detect Power Down mode, QSGMII up	92	30	0.1	180
4 ports + QSGMII, Software Power Down mode, QSGMII up	81	25	0.1	156
4 ports + QSGMII, Software Power Down mode, QSGMII down	26	10	0.1	56
4 ports + QSGMII, hardware reset	15	17	0.1	58

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6.3.2 WORST-CASE FOUR PORT OPERATION

All worst-case measurements were taken at +5% power supply and +125°C junction temperature.

TABLE 6-4: WORST-CASE FOUR PORT (1.27V, 3.465V, 3.465V) POWER CONSUMPTION

Device Conditions	1.27V Total (mA) (Note 6-3)	3.465V VDD_{AH} Total (mA) (Note 6-4)	3.465V VDD_{IO} Total (mA) (Note 6-5)	Total Device Power (mW)
4 ports + QSGMII, 1000BASE-T Master link-up, no traffic	849.6	559.2	9.5	3050
4 ports + QSGMII, 1000BASE-T Slave link-up, No traffic	850.6	559.1	9.5	3051
4 ports + QSGMII, 100BASE-TX link-up, no traffic	325.9	271.4	13.2	1401
4 ports + QSGMII, 10BASE-T link-up, no traffic	175.5	228	21.5	1088
4 ports + QSGMII, 10BASE-Te link-up, no traffic	175.8	228.6	21.8	1091
4 ports + QSGMII, 1000BASE-T Master full-duplex, 100% utilization	872	557.4	5.5	3058
4 ports + QSGMII, 1000BASE-T Slave full-duplex, 100% utilization	878.5	557.4	5.3	3066
4 ports + QSGMII, 100BASE-TX full-duplex, 100% utilization	319.3	271.5	7.6	1373
4 ports + QSGMII, 10BASE-T full-duplex, 100% utilization	172.2	283.5	11.2	1240
4 ports + QSGMII, 10BASE-Te full-duplex, 100% utilization	172.4	284	11.2	1242
4 ports + QSGMII, 1000BASE-T Master, EEE Sleep state	395.3	373.5	8.6	1827
4 ports + QSGMII, 1000BASE-T Slave, EEE Sleep state	395.3	373.2	8.6	1825
4 ports + QSGMII, 100BASE-TX, EEE Sleep state	234.5	256.3	13.2	1232
4 ports + QSGMII, Energy Detect Power Down mode, QSGMII up	199.5	33.8	0.1	371
4 ports + QSGMII, Software Power Down mode, QSGMII up	137.5	27.5	0.1	271
4 ports + QSGMII, Software Power Down mode, QSGMII down	83.2	12.4	1.2	153
4 ports + QSGMII, hardware reset	67.5	18.2	1.3	154

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TABLE 6-5: WORST-CASE FOUR PORT (1.27V, 2.625V, 2.625V) POWER CONSUMPTION

Device Conditions	1.27V Total (mA) (Note 6-3)	2.625V VDD_{AH} Total (mA) (Note 6-4)	2.625V VDD_{IO} Total (mA) (Note 6-5)	Total Device Power (mW)
4 ports + QSGMII, 1000BASE-T Master link-up, No traffic	853	505.5	4.3	2422
4 ports + QSGMII, 1000BASE-T Slave link-up, no traffic	858.4	505.9	4.3	2430
4 ports + QSGMII, 100BASE-TX link-up, no traffic	333.7	245.3	6.3	1085
4 ports + QSGMII, 10BASE-T link-up, no traffic	180.3	202.4	10.4	788
4 ports + QSGMII, 10BASE-Te link-up, no traffic	180.6	202.5	10.5	789
4 ports + QSGMII, 1000BASE-T Master full-duplex, 100% utilization	878.4	504.9	2.3	2447
4 ports + QSGMII, 1000BASE-T Slave full-duplex, 100% utilization	879.2	504.1	2.2	2446
4 ports + QSGMII, 100BASE-TX full-duplex, 100% utilization	331.5	245.6	6.4	1083
4 ports + QSGMII, 10BASE-T full-duplex, 100% utilization	180.1	202.3	10.4	788
4 ports + QSGMII, 10BASE-Te full-duplex, 100% utilization	180.8	202.7	10.4	790
4 ports + QSGMII, 1000BASE-T Master, EEE Sleep state	306.4	389.2	4.0	1422
4 ports + QSGMII, 1000BASE-T Slave, EEE Sleep state	306.1	389.5	4.0	1422
4 ports + QSGMII, 100BASE-TX, EEE Sleep state	218.3	273	6.0	1010
4 ports + QSGMII, Energy Detect Power Down mode, QSGMII up	158.1	30.5	0.1	282
4 ports + QSGMII, Software Power Down mode, QSGMII up	136.8	26.7	0.1	244
4 ports + QSGMII, Software Power Down mode, QSGMII down	85.6	10	0.1	136
4 ports + QSGMII, hardware reset	71.3	16.7	0.7	137

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TABLE 6-6: WORST-CASE FOUR PORT (1.27V, 2.625V, 1.89V) POWER CONSUMPTION

Device Conditions	1.27V Total (mA) (Note 6-3)	2.625V VDD_{AH} Total (mA) (Note 6-4)	1.89V VDD_{IO} Total (mA) (Note 6-5)	Total Device Power (mW)
4 ports + QSGMII, 1000BASE-T link-up, no traffic	850.2	505.2	1.0	2408
4 ports + QSGMII, 1000BASE-T Slave link-up, No traffic	850	505.4	1.0	2409
4 ports + QSGMII, 100BASE-TX link-up, no traffic	333.7	245.3	1.0	1070
4 ports + QSGMII, 10BASE-T link-up, no traffic	180.3	202.4	1.6	764
4 ports + QSGMII, 10BASE-Te link-up, no traffic	180.5	202.5	1.6	764
4 ports + QSGMII, 1000BASE-T Master full-duplex, 100% utilization	878.4	504.9	0.7	2443
4 ports + QSGMII, 1000BASE-T full-duplex, 100% utilization	877.8	504.1	0.7	2440
4 ports + QSGMII, 100BASE-TX full-duplex, 100% utilization	331.1	245.6	0.7	1067
4 ports + QSGMII, 10BASE-T full-duplex, 100% utilization	179.8	202.3	1.0	762
4 ports + QSGMII, 10BASE-Te full-duplex, 100% utilization	180.4	202.7	1.0	764
4 ports + QSGMII, 1000BASE-T, EEE Sleep state	260.5	380.3	1.1	1331
4 ports + QSGMII, 1000BASE-T Slave, EEE Sleep state	260.7	380.2	1.1	1331
4 ports + QSGMII, 100BASE-TX, EEE Sleep state	207.6	219.5	1.5	843
4 ports + QSGMII, Energy Detect Power Down mode, QSGMII up	145.8	29.7	0.0	264
4 ports + QSGMII, Software Power Down mode, QSGMII up	103.2	25.5	0.2	199
4 ports + QSGMII, Software Power Down mode, QSGMII down	85.4	10	0.2	136
4 ports + QSGMII, hardware reset	71	16.7	0.3	135

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6.4 Package Thermal Specifications

TABLE 6-7: PACKAGE THERMAL PARAMETERS

Parameter	Symbol	Value	Units	Description
Thermal Resistance Junction to Ambient	Θ_{JA}	16.72	°C/W	Measured in still air
		13.67	°C/W	Airflow 1 m/s
		12.76	°C/W	Airflow 2.5 m/s
Thermal Resistance Junction to Bottom of Case	Ψ_{JT}	0.11	°C/W	Measured in still air
Thermal Resistance Junction to Top of Case	Θ_{JC}	2.44	°C/W	—
Thermal Resistance Junction to Board	Θ_{JB}	5.36	°C/W	
Thermal Parameter Junction to Board	Ψ_{JB}	5.45	°C/W	Measured in still air

Note: Thermal parameters are measured or estimated for devices in a multi-layer 2S2P PCB per JESD51.

6.5 DC Specifications

TABLE 6-8: NON-VARIABLE I/O DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit	Note
ICLK Type Input Buffer						Note 6-6
Low Input Level	V_{IL}	—	—	0.5	V	
High Input Level	V_{IH}	2.0	—	—	V	
Input Leakage	I_{IH}	-10	—	10	µA	
LVDS1 Type Input Buffer						Note 6-7
Input Common mode Voltage Range	V_{CM}	$V_{ID}/2$	—	$2.4-V_{ID}/2$	V	
Input Peak Diff. Voltage	V_{ID}	100	—	600	mV	
LVDS2 Type Input Buffer						Note 6-7
Input Common mode Voltage Range	V_{CM}	0	—	1.1	V	
Input Peak Diff. Voltage	V_{ID}	300	—	—	mV	

Note 6-6 XI can optionally be driven from a 25 MHz single-ended clock oscillator to which these specifications apply.

Note 6-7 The maximum input frequency for LVDS1/LVDS2 pins is 150 MHz.

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TABLE 6-9: VARIABLE I/O DC ELECTRICAL CHARACTERISTICS VDDIO = 3.3V/2.5V/1.8V

Parameter	Symbol	Min	Typ 1.8	Typ 2.5	Typ 3.3	Max	Unit	Note
VIS Type Input Buffer								
Low Input Level	V_{IL}	—	—	—	—	0.39x**VDDIO**	V	
High Input Level	V_{IH}	0.63x**VDDIO**	—	—	—		V	
Schmitt Falling Trip Point	V_{T-}	0.67	0.8	1.1	1.46	1.68	V	
Schmitt Rising Trip Point	V_{T+}	0.8	0.94	1.25	1.62	1.85	V	
Schmitt Trigger Hysteresis (V_{IHT} - V_{ILT})	V_{HYS}	109.9	149	148	164	219.4	mV	
Input Leakage (V_{IN} = **P_VSS** or **VDDIO**)	I_{IH}	-10	—	—	—	10	µA	Note 6-8
Input Capacitance (generic guess)	C_{IN}	—	—	—	—	3	pF	
Effective Pull-Up Resistance (V_{IN} = **P_VSS**)	R_{PU}	58.9	70	—	—	83.7	kΩ	
Effective Pull-Down Resistance (V_{IN} = **VDDIO**)	R_{PD}	58.7	70	—	—	84.5	kΩ	
VO12 Type Buffer								
Low Output Level	V_{OL}	—		—		0.4	V	I_{OL} = -12 mA
High Output Level	V_{OH}	**VDDIO**-0.4		—		—	V	I_{OH} = 12 mA
Output Tri-State Leakage	I_{OZ}	-10		—		10	µA	Note 6-8
VOD12 Type Buffer								
Low Output Level	V_{OL}	—		—		0.4	V	I_{OL} = -12 mA
Output Tri-State Leakage	I_{OZ}	-10		—		10	µA	Note 6-8
VOS12 Type Buffer								
High Output Level	V_{OH}	**VDDIO**-0.4		—		—	V	I_{OH} = 12 mA
Output Tri-State Leakage	I_{OZ}	-10		—		10	µA	Note 6-8

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TABLE 6-9: VARIABLE I/O DC ELECTRICAL CHARACTERISTICS VDDIO = 3.3V/2.5V/1.8V

Parameter	Symbol	Min	Typ 1.8	Typ 2.5	Typ 3.3	Max	Unit	Note
SRL Type Input Buffer								—
Low Input Level	V_{IL}	—	—	—	—	0.4x**VDDIO**	V	
High Input Level	V_{IH}	0.6x**VDDIO**	—	—	—	—	V	
Schmitt Falling Trip Point	V_{T-}	0.76	0.90	1.11	1.42	1.64	V	
Schmitt Rising Trip Point	V_{T+}	0.85	0.99	1.23	1.55	1.76	V	
Schmitt Trigger Hysteresis (V_{IHT} - V_{ILT})	V_{HYS}	60	90	121	127	150	mV	
Input Leakage (V_{IN} = **P_VSS** or **VDDIO**)	I_{IH}	-15	—	—	—	15	µA	
Input Capacitance	C_{IN}	—	—	—	—	3	pF	
SRL Type Output Buffer								
Low Output Level	V_{OL}	—	—	—	—	0.4	V	I_{OL} = -5 mA
High Output Level	V_{OH}	**VDDIO**-0.4	—	—	—	—	V	I_{OH} = 5 mA
Output Impedance	R_O	—	50	50	50	—	Ω	—

Note 6-8 This specification applies to all inputs without pull-ups or pull-downs and three-stated bi-directional pins.

TABLE 6-10: 1000BASE-T TRANSCEIVER CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Peak Differential Output Voltage IEEE 802.3 clause 40.6.1.2.1	V_{OP}	670	—	820	mV	Note 6-9
Signal Amplitude Symmetry IEEE 802.3 clause 40.6.1.2.1	V_{SS}	—	—	1	%	Note 6-9
Signal Scaling IEEE 802.3 clause 40.6.1.2.1	V_{SC}	—	—	2	%	Note 6-10
Output Droop IEEE 802.3 clause 40.6.1.2.2	V_{OD}	73.1	—	—	%	Note 6-9
Transmission Distortion IEEE 802.3 clause 40.6.1.2.4	—	—	—	10	mV	Note 6-11

Note 6-9 IEEE 802.3 clause 40.6.1.1.2 Test Mode 1

Note 6-10 From 1/2 of average V_{OP}, Test Mode 1

Note 6-11 IEEE 802.3 clause 40.6.1.1.2 distortion processing

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TABLE 6-11: 100BASE-TX TRANSCEIVER CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Peak Differential Output Voltage ANSI X3.263 clause 9.1.2.2	V_{OUT}	±0.95	—	±1.05	V	Note 6-12
Signal Amplitude Symmetry ANSI X3.263 clause 9.1.4	V_{SS}	—	—	2	%	Note 6-12
Signal Rise and Fall Time ANSI X3.263 clause 9.1.6	T_{RF}	3	—	5	ns	Note 6-12
Rise and Fall Symmetry ANSI X3.263 clause 9.1.6	T_{RFS}	0	—	0.5	ns	Note 6-12
Duty Cycle Distortion ANSI X3.263 clause 9.1.8	D_{CD}	—	—	±0.25	ns	Note 6-13
Overshoot and Undershoot ANSI X3.263 clause 9.1.3	V_{OS}	—	—	5	%	—
Output Jitter ANSI X3.263 clause 9.1.9	—	—	0.7	1.4	ns	Note 6-14
Reference Voltage of **ISET** (using 6.04kΩ - 1% resistor)	V_{SET}	—	0.61	—	V	—

Note 6-12 Measured at line side of transformer, line replaced by 100Ω (±1%) resistor.

Note 6-13 Offset from 16 ns pulse width at 50% of pulse peak.

Note 6-14 Peak to Peak, measured differentially.

TABLE 6-12: 10BASE-T/10BASE-Te TRANSCEIVER CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Transmitter Peak Differential Output Voltage IEEE 802.3 clause 14.3.1.2.1	V_{OUT} 10BASE-T	2.2	2.5	2.8	V	Note 6-15
	V_{OUT} 10BASE-Te	1.54	—	1.96	V	Note 6-15
Output Jitter IEEE 802.3 clause 14.3.1.2.3	—	—	1.8	3.5	ns	Note 6-16
Signal Rise and Fall Time	T_{RF}	—	25	—	ns	—
Receiver Differential Squelch Threshold IEEE 802.3 clause 14.3.1.3.2	V_{DS}	300	400	—	mV	Note 6-17

Note 6-15 Measured with 100Ω resistive load.

Note 6-16 Measured differentially following the twisted-pair model with a 100Ω resistive load.

Note 6-17 5 MHz square wave.

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TABLE 6-13: POR THRESHOLDS

POR	Conditions	Rising Threshold (Volts)			Falling Threshold (Volts)			Hysteresis (Millivolts)		
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
1.21V Ethernet PHY Analog (**VDDAL**)	**VDDAH** = 2.5V	0.73	0.76	0.80	0.64	0.68	0.80	0	80	114
	VDDAH = 3.3V	0.73	0.76	0.82	0.63	0.70	0.82	0	65	120
2.5V/3.3V Ethernet PHY Analog (**VDDAH**)	—	1.9	2.1	2.2	1.9	2.0	2.1	65	110	145
1.21V Digital Core (**VDDCORE**)	**VDDIO** = 1.8V Rise/Fall = 10 µs	0.913	0.929	0.948	0.65	0.68	0.706	0.217	0.248	0.295
	VDDIO = 1.8V Rise/Fall = 10 ms	0.853	0.862	0.876	0.737	0.749	0.758	0.107	0.112	0.122
	VDDIO = 2.5V Rise/Fall = 10 µs	0.916	0.933	0.954	0.644	0.677	0.704	0.221	0.256	0.308
	VDDIO = 2.5V Rise/Fall = 10 ms	0.853	0.862	0.877	0.737	0.749	0.757	0.107	0.112	0.123
	VDDIO = 3.3V Rise/Fall = 10 µs	0.918	0.937	0.962	0.638	0.672	0.701	0.226	0.265	0.322
	VDDIO = 3.3V Rise/Fall = 10 ms	0.853	0.862	0.877	0.737	0.749	0.757	0.107	0.112	0.123
3.3V/2.5V/1.8V Variable I/O (**VDDIO**)	**VDDIO** = 1.8V Rise/Fall = 10 µs	1.62	1.8	1.98	0.815	0.997	1.167	0.453	0.802	1.164
	VDDIO = 1.8V Rise/Fall = 10 ms	1.454	1.47	1.491	1.218	1.231	1.262	0.212	0.238	0.243
	VDDIO = 2.5V Rise/Fall = 10 µs	2.02	2.17	2.67	0.8	0.986	1.159	0.88	1.183	1.81
	VDDIO = 2.5V Rise/Fall = 10 ms	1.454	1.47	1.491	1.216	1.23	1.261	0.213	0.240	0.245
	VDDIO = 3.3V Rise/Fall = 10 µs	2.15	2.34	3.0	0.645	0.973	1.152	1.0	1.373	2.16
	VDDIO = 3.3V Rise/Fall = 10 ms	1.455	1.47	1.491	1.215	1.228	1.26	0.214	0.242	0.247

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6.6 AC Specifications

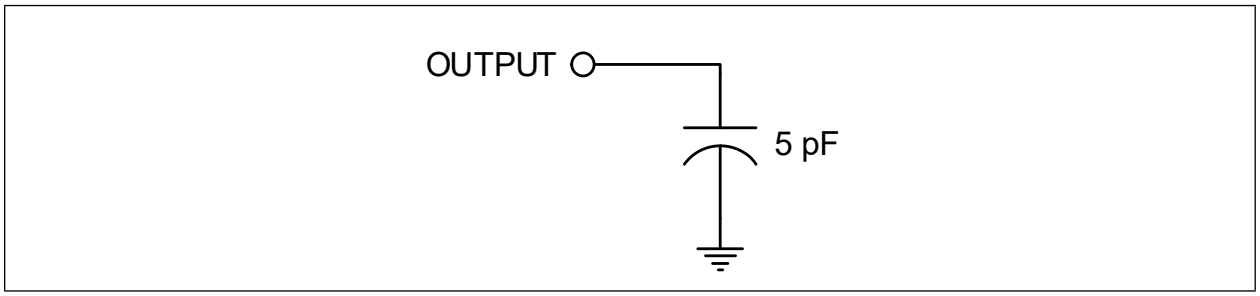
This section details the various AC timing specifications of the device.

Note:	The QSGMII timing adheres to the QSGMII Specification. Refer to the QSGMII Specification Rev. 1.3 (EDCS-540123) [4] for additional QSGMII timing information.

6.6.1 EQUIVALENT TEST LOAD

Output timing specifications assume a 5 pF equivalent test load, unless otherwise noted, as illustrated in Figure 6-1.

FIGURE 6-1: OUTPUT EQUIVALENT TEST LOAD

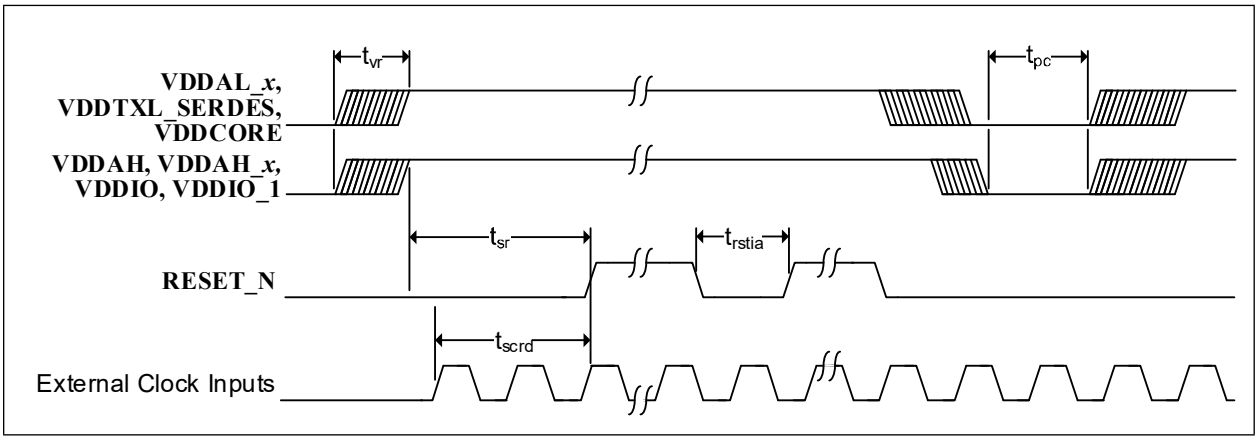


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6.6.2 POWER SEQUENCE TIMING

This diagram illustrates the device power sequencing requirements.

FIGURE 6-2: POWER SEQUENCE TIMING INTERNAL REGULATORS



There is no power sequence requirement between transceiver (**VDDAH**, **VDDAH_*x***), 1.1V core (**VDDCORE**, **VDDAL_*x***, **VDDTXL_SERDES**), and digital I/O (**VDDIO**, **VDDIO_1**) power rails.

The power-up waveforms must be monotonic for all supply voltages to the device.

RESET_N must be held asserted following stable voltages for the minimum period specified and if re-asserted, for the minimum period specified.

Before the next power-up cycle, all supply voltages to the device must reach less than 0.4V and there must be a minimum wait time of 150 ms from power-off to power-on.

TABLE 6-14: POWER SEQUENCING TIMING VALUES

Symbol	Description	Min	Typ	Max	Unit
t_{vr}	Supply voltages rise time (must be monotonic)	0.1	—	100	ms
t_{sr}	Stable supply voltages to de-assertion of reset	100	—	—	ms
t_{rstia}	**RESET_N** input assertion time	1	—	—	µs
t_{scrd}	Stable external clock references to de-assertion of reset	10	—	—	ms
t_{pc}	Supply voltages cycle off-to-on time	150	—	—	ms

6.6.3 RESET PIN CONFIGURATION STRAP TIMING

Figure 6-3 illustrates the **RESET_N** timing requirements and its relation to the configuration straps. **RESET_N** must be asserted for the minimum period specified.

FIGURE 6-3: RESET_N CONFIGURATION STRAP TIMING

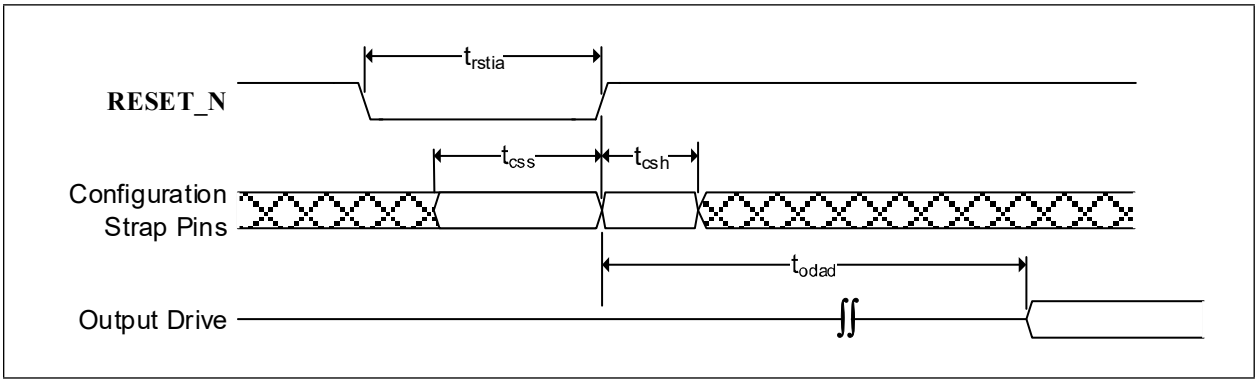


TABLE 6-15: RESET_N CONFIGURATION STRAP TIMING

Symbol	Description	Min	Typ	Max	Unit
t_{rstia}	**RESET_N** input assertion time	1	—	—	µs
t_{css}	Configuration strap setup before **RESET_N** de-assertion	5	—	—	ns
t_{csh}	Configuration strap hold after **RESET_N** de-assertion	5	—	—	ns
t_{odad}	Output drive after **RESET_N** de-assertion	3.5	—	—	µs

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6.6.4 AUTO-NEGOTIATION FAST LINK PULSE (FLP) TIMING

FIGURE 6-4: AUTO-NEGOTIATION FLP TIMING

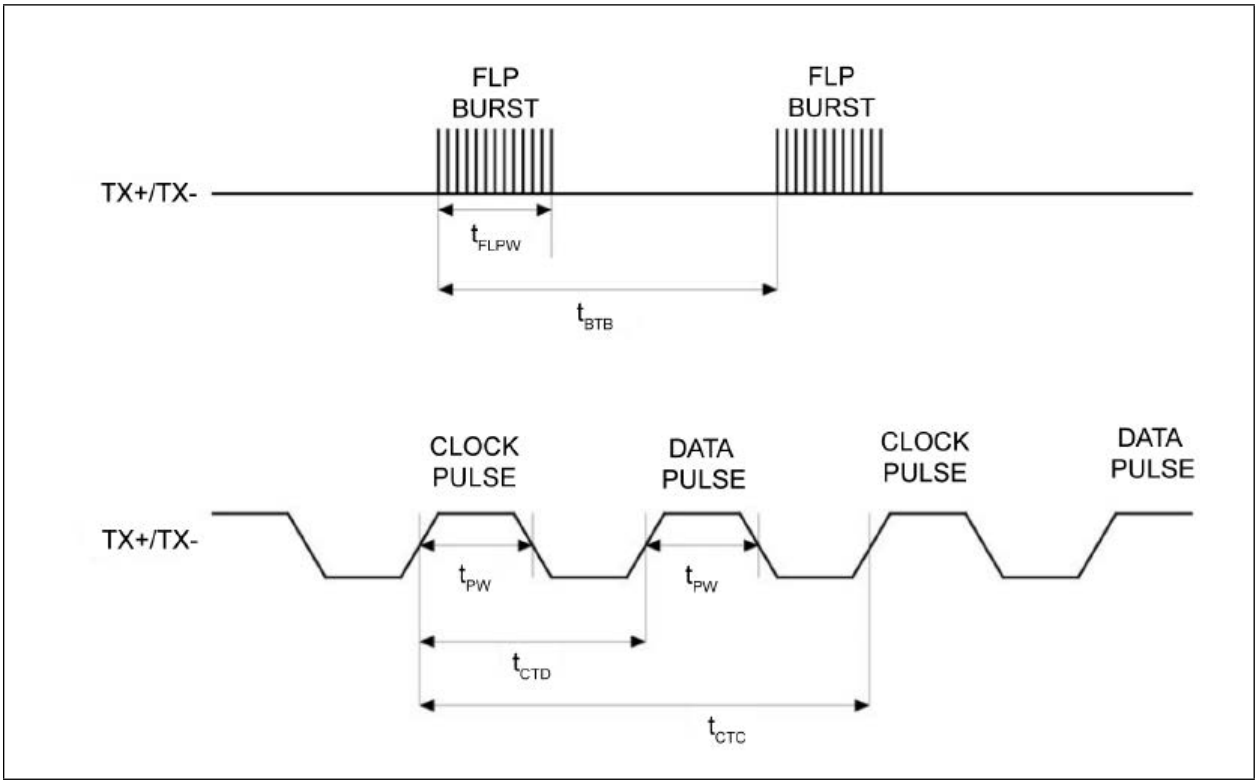


TABLE 6-16: AUTO-NEGOTIATION FLP TIMING PARAMETERS

Symbol	Description	Min	Typ	Max	Unit
t_{BTB}	FLP burst to FLP burst	8	16	24	ms
t_{FLPW}	FLP burst width	–	2	–	ms
t_{PW}	Clock/Data pulse width	–	100	–	ns
t_{CTD}	Clock pulse to data pulse	55.5	64	69.5	µs
t_{CTC}	Clock pulse to clock pulse	111	128	139	µs
	Number of clock/data pulses per FLP burst	17	–	33	–

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6.6.5 MDC/MDIO TIMING

This section specifies the MDC/MDIO timing of the device. These timing numbers are valid for high-speed MDIO operation using push-pull MDIO buffers.

FIGURE 6-5: MDC/MDIO TIMING

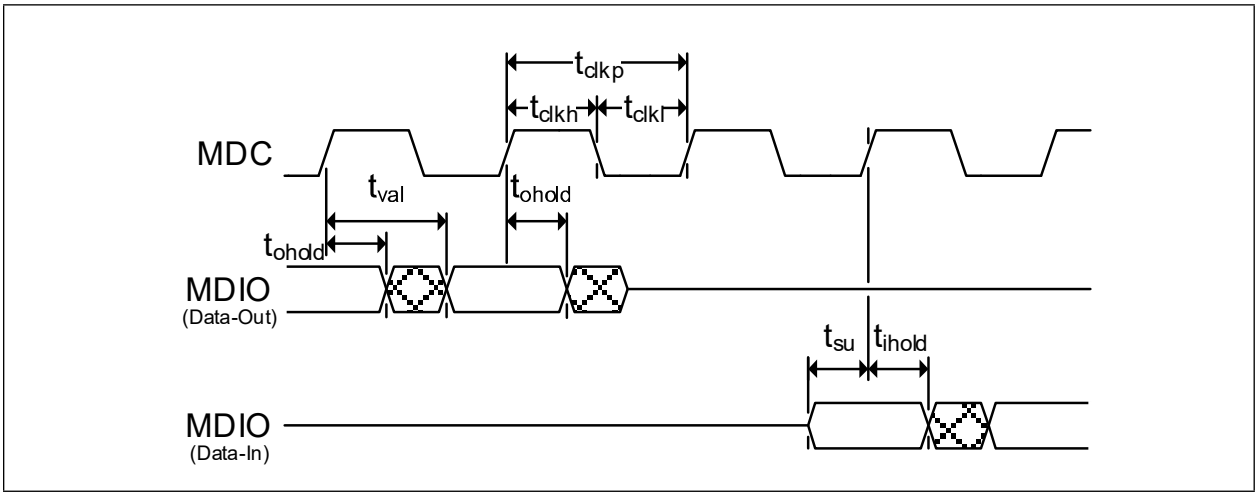


TABLE 6-17: MDC/MDIO TIMING VALUES

Symbol	Description	Min	Typ	Max	Unit
t_{clkp}	**MDC** period	40	—	Note 6-18	ns
t_{clkh}	**MDC** high time	10	—	—	ns
t_{clkl}	**MDC** low time	10	—	—	ns
t_{val}	**MDIO** (read from PHY) output valid from rising **MDIO** of **MDC**	—	—	20	ns
t_{ohold}	**MDIO** (read from PHY) output hold from rising edge of **MDC**	4	—	—	ns
t_{su}	**MDIO** (write to PHY) input setup time to rising edge of **MDC**	8 Note 6-19	—	—	ns
t_{ihold}	**MDIO** (write to PHY) input hold time after rising edge of **MDC**	8 Note 6-19	—	—	ns

Note 6-18 The device can operate with **MDC** clock frequencies generated from bit banging in the 10s/100s of Hertz.

Note 6-19 These values provide 2 ns margin beyond the IEEE specification.

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6.6.6 JTAG TIMING

This section specifies the JTAG timing of the device.

FIGURE 6-6: JTAG TIMING

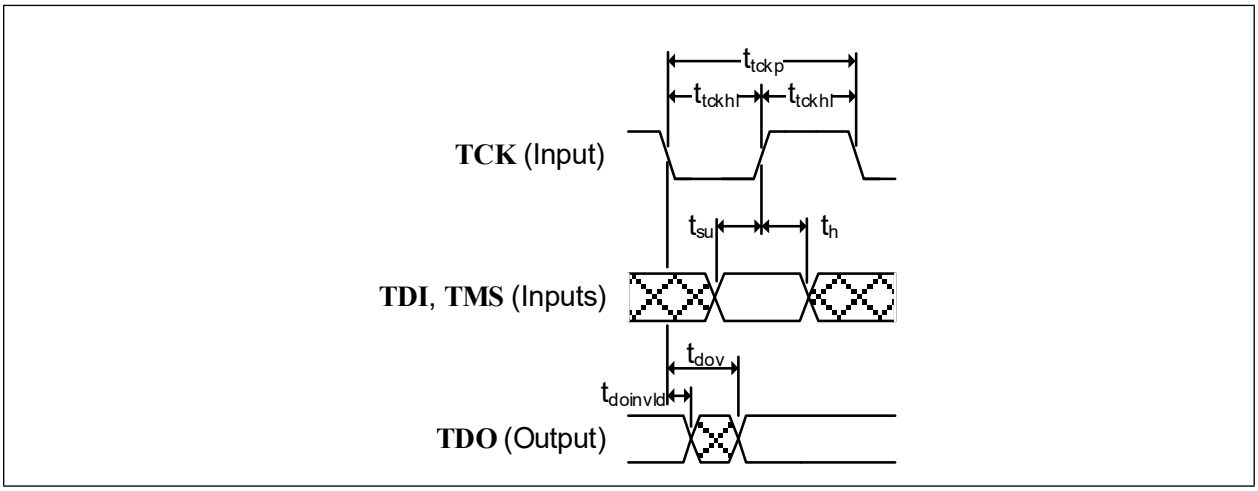


TABLE 6-18: JTAG TIMING VALUES

Symbol	Description	Min	Max	Unit	Note
t_{tckp}	**TCK** clock period	40	—	ns	—
t_{tckhl}	**TCK** clock high/low time	t_{tckp}*0.4	t_{tckp}*0.6	ns	
t_{su}	**TDI**, **TMS** setup to **TCK** rising edge	15	—	ns	
t_h	**TDI**, **TMS** hold from **TCK** rising edge	4	—	ns	
t_{dov}	**TDO** output valid from **TCK** falling edge	—	16	ns	
$t_{doinvld}$	**TDO** output invalid from **TCK** falling edge	0	—	ns	

Note: Timing values are with respect to an equivalent test load of 25 pF.

6.6.7 GPIO TIMING

This section specifies the general GPIO timing of the device.

TABLE 6-19: GPIO TIMING VALUES

Symbol	Description	Min	Typ	Max	Unit
t_{input_pulse}	GPIO input pulse width	18	—	—	ns
t_{output_pulse}	GPIO output pulse width	14	—	—	ns
t_{input_su}	GPIO input setup/hold timing	N/A, treat as asynchronous (Note 6-20)			
t_{output_hold}	GPIO output valid/hold timing	N/A, treat as asynchronous (Note 6-20)			

Note 6-20 GPIOs must have pulse widths with a minimum of two 125 MHz clocks, but no synchronous timing relationship is specified. GPIOs configured as alternate functions may have synchronous timing relationships.

6.6.8 GPIO SOF DETECTION TIMING

This section specifies the GPIO SOF timing of the device.

FIGURE 6-7: GPIO SOF TIMING

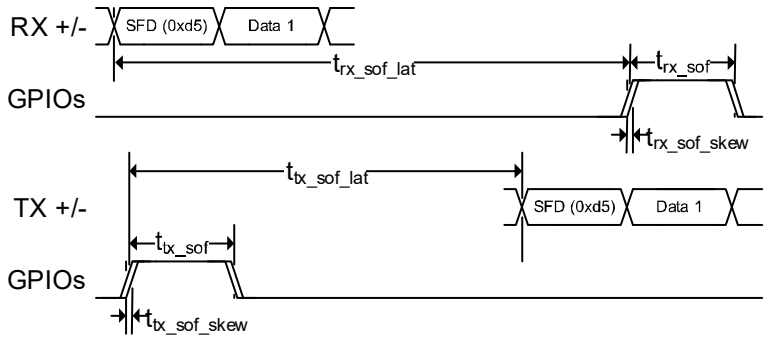


TABLE 6-20: GPIO SOF TIMING VALUES

Symbol	Description		Min	Typ	Max	Unit
$t_{rx_sof_lat}$	RX SOF latency	1000M 100M 10M	—	472 456 7696	—	ns
t_{rx_sof}	RX SOF pulse width		—	Note 6-21	—	ns
$t_{rx_sof_skew}$	RX SOF skew between GPIOs		—	0.5	1	ns
$t_{tx_sof_lat}$	TX SOF latency	1000M 100M 10M	—	59 150 645	—	ns
t_{tx_sof}	TX SOF pulse width		—	Note 6-21	—	ns
$t_{tx_sof_skew}$	TX SOF skew between GPIOs		—	0.5	1	ns

Note 6-21 8 ns for 1000BASE-T operation, 40 ns for 100BASE-TX operation, 400 ns for 10BASE-T operation.

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6.6.9 CK25OUT TIMING

This section specifies the **CK25OUT** reference clock timing of the device.

- Duty Cycle: (40% minimum, 50% typical, 60% maximum)
- Jitter: < 100 ps rms

6.6.10 CK125_REF_INP/M TIMING

This section specifies the **CK125_REF_INP/M** reference clock timing of the device.

- Duty Cycle: (40% minimum, 50% typical, 60% maximum)
- Jitter: < 100 ps rms
- Frequency: 125 MHz ± 50 ppm

6.7 Clock Circuit

The device can accept either a 25 MHz crystal (preferred) or a 25 MHz single-ended clock oscillator (± 50 ppm, max jitter 100 ps rms) input. If the single-ended clock oscillator method is implemented, **XO** must be left unconnected and **XI** must be driven with a nominal 0-3.3V clock signal. The input clock duty cycle is 40% minimum, 50% typical and 60% maximum.

It is recommended that a crystal utilizing matching parallel load capacitors be used for the crystal input/output signals (**XI/XO**). See Table 6-21 for the recommended crystal specifications.

TABLE 6-21: CRYSTAL SPECIFICATIONS

Parameter	Symbol	Min	Nom	Max	Unit	Note
Crystal Cut	AT, typ					—
Crystal Oscillation Mode	Fundamental Mode					
Crystal Calibration Mode	Parallel Resonant Mode					
Frequency	F_{fund}	—	25.000	—	MHz	
Frequency Tolerance @ 25°C	F_{tol}	—	—	±50	ppm	Note 6-22
Frequency Stability Over Temp	F_{temp}	—	—	±50	ppm	Note 6-22
Frequency Deviation Over Time	F_{age}	—	±3 to 5	—	ppm	Note 6-23
Total Allowable PPM Budget		—	—	±50	ppm	Note 6-24
Shunt Capacitance	C_O	—	—	6	pF	—
Load Capacitance	C_L	—	—	25	pF	
Motional Inductance	LM	—	—	10	mH	
Drive Level	P_W	—	—	100	µW	
Equivalent Series Resistance	R_1	—	—	50	Ohm	
Operating Temperature Range	—	Note 6-25	—	Note 6-26	°C	
XI Pin Capacitance	—	-—	2 typ	—	pF	Note 6-27
XO Pin Capacitance	—	—	2 typ	—	pF	Note 6-27
Crystal Startup Time	t_{XSO}	<2			ms	—

Note 6-22 The maximum allowable values for Frequency Tolerance and Frequency Stability are application dependent. Since any particular application must meet the IEEE ±50 ppm Total PPM Budget, the combination of these two values must be approximately ±45 ppm (allowing for aging).

Note 6-23 Frequency Deviation Over Time is also referred to as Aging.

Note 6-24 The total deviation for the Transmitter Clock Frequency is specified by IEEE 802.3u as ±50 ppm.

Note 6-25 0°C ambient for commercial version, -40°C ambient for industrial version.

Note 6-26 +85°C ambient.

Note 6-27 This number includes the pad, the bond wire and the lead frame. PCB capacitance is not included in this value. The **XO/XI** pin and PCB capacitance values are required to accurately calculate the value of the two external load capacitors. These two external load capacitors determine the accuracy of the 25.000 MHz frequency.

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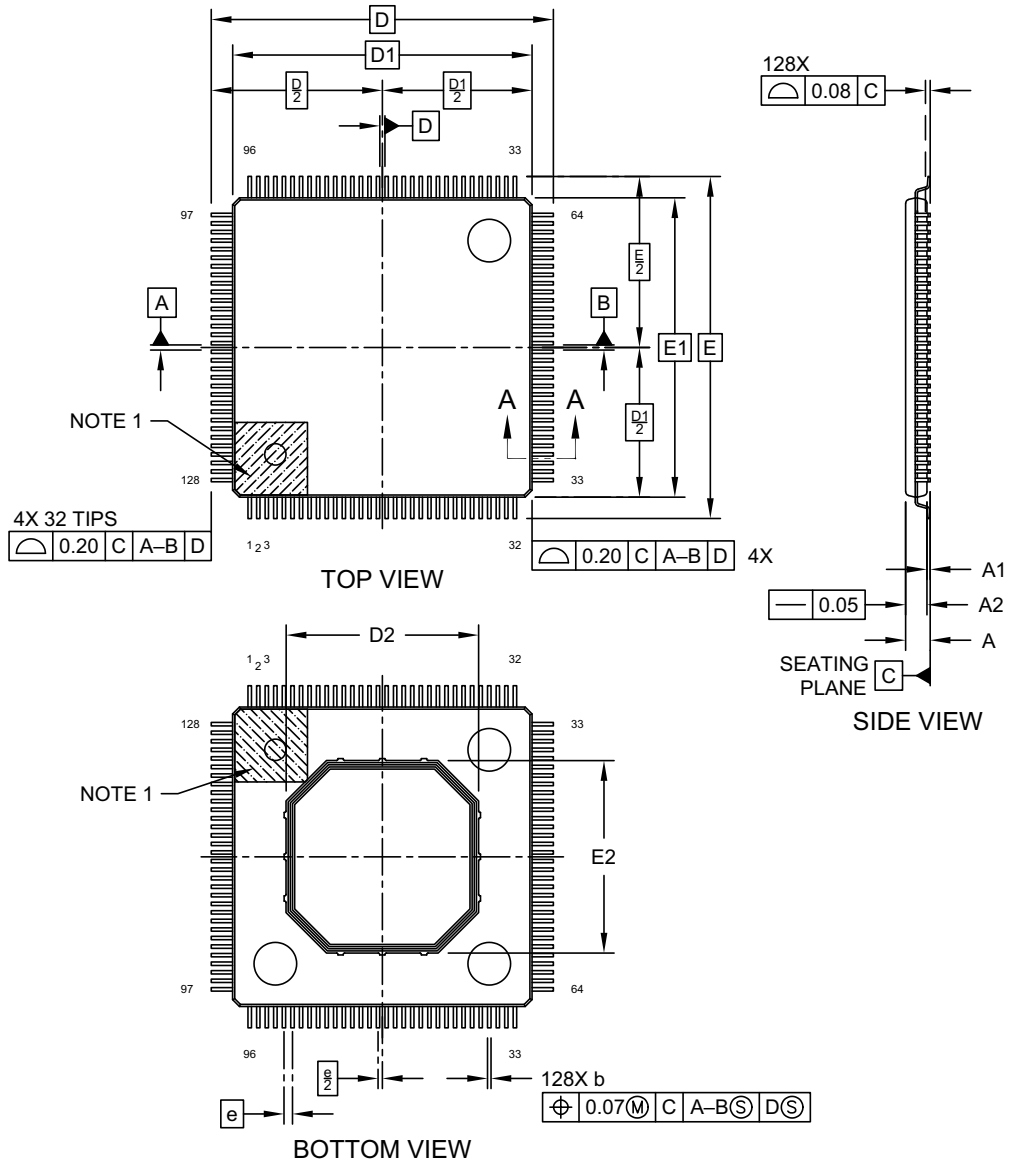
7.0 PACKAGE OUTLINE

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

FIGURE 7-1: 128-TQFP PACKAGE (DRAWING)

128-Lead Thin Quad Flat Pack (ZMX) - 14x14x1.0 mm Body [TQFP]
With 9x9 mm Grooved Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

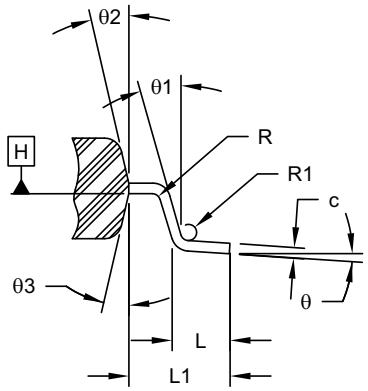


Microchip Technology Drawing C04-502 Rev B Sheet 1 of 2

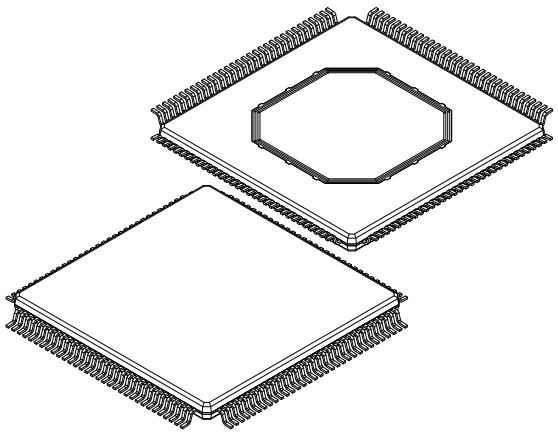
FIGURE 7-2: 128-TQFP PACKAGE (DIMENSIONS)

128-Lead Thin Quad Flat Pack (ZMX) - 14x14x1.0 mm Body [TQFP]
With 9x9 mm Grooved Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A-A



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		128	
Lead Pitch	e		0.40 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.05	0.10	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Overall Length	D		16.00 BSC	
Molded Package Length	D1		14.00 BSC	
Exposed Pad Length	D2	8.90	9.00	9.10
Overall Width	E		16.00 BSC	
Molded Package Width	E1		14.00 BSC	
Exposed Pad Width	E2	8.90	9.00	9.10
Lead Width	b	0.13	0.16	0.23
Lead Thickness	c	0.09	-	0.20
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	θ	0°	-	7°
Lead Angle	θ1	0°	-	-
Mold Draft Angle Top	θ2	11°	12°	13°
Mold Draft Angle Bottom	θ3	11°	12°	13°
Lead Bend Radius	R	0.08	-	-
Lead Bend Radius	R1	0.08	-	0.20

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

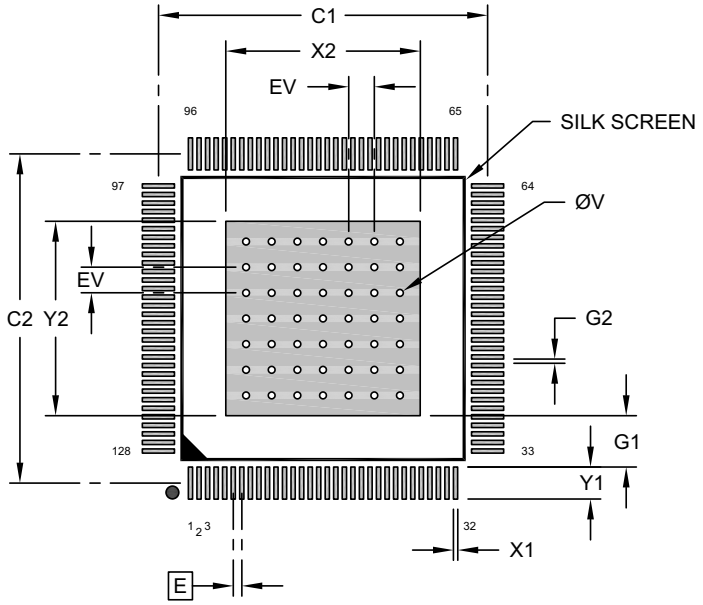
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FIGURE 7-3: 128-TQFP PACKAGE (LAND PATTERN)

128-Lead Thin Quad Flat Pack (ZMX) - 14x14x1.0 mm Body [TQFP]
With 9x9 mm Grooved Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	X2			9.10
Optional Center Pad Length	Y2			9.10
Contact Pad Spacing	C1		15.40	
Contact Pad Spacing	C2		15.40	
Contact Pad Width (X128)	X1			0.20
Contact Pad Length (X128)	Y1			1.50
Contact Pad to Center Pad (X128)	G1	2.40		
Contact Pad to Contact Pad (X124)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2502 Rev B

APPENDIX A: DOCUMENT REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00003591J (08-07-25)	Throughout Document.	• Miscellaneous grammatical and formatting changes.
	Throughout Document.	• Digital Core (VDDCORE) and Analog Operation (VDDAL) updated from “1.1V” to “1.21V”.
	Section 3.3.1, Device Mode Select (MODE_SEL[4:0])	• Removed “preliminary and subject to change” note regarding MODE_SEL[4:0] function.
	Section 7.0, Package Outline	• Updates made to Package Drawing, Dimensions, and Land Pattern.
DS00003591H (12-05-24)	Throughout Document.	• LDO Controller has been defeatured. Sections detailing its operation have been removed or updated. See below for further details.
	Table 3-5, "Miscellaneous Pins"	• Description for LDO Controller Output (LDO_O) has been changed from: “On-chip +1.1V LDO controller output. This pin drives the input gate of a P-channel MOSFET to generate +1.1V for the device’s core voltages. Note: If the system provides 1.1V, this pin is not used and can be left unconnected.” to: “On-chip +1.1V LDO controller output. This functionality has been defeatured. The pin should be left unconnected. Please refer to the errata for further details.”
	Section 4.1, "Voltage Regulator and Power Connections"	• This section have been modified. Text changed from: “The LAN8804 integrates an optional LDO controller for use with an external P-channel MOSFET to generate the 1.1V supply from an existing 2.5V or 3.3V source. Use of the LDO controller and MOSFET is not required. An external 1.1V supply can be alternatively utilized.” to: “The LAN8804 has an integrated LDO controller. This controller has been defeatured. Please refer to the errata for further details.”
	Section 4.1.1, "LDO Disable"	• This section have been modified. Text changed from: “The LDO controller is enabled by default. It may alternatively be disabled via internal register settings. An external source of 1.1V is necessary if the LDO is disabled.” to: “The LDO has been defeatured and **LDO_O** should be left disconnected. Microchip recommends disabling the LDO output by setting the active low LDO enable bit in the Analog Control Register 11. An external source of 1.21V is required for operation.”

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TABLE A-1: REVISION HISTORY (CONTINUED)

Revision	Section/Figure/Entry	Correction
	Figure 4-1, "Power Connections"	• Figure modified to remove LDO and replace with 1.21V source.
	Table 5-1, "MDI/MDI-X Pin Mapping"	• Corrected MDI/MDI-X Pin Mapping names and designations
	Section 5.19.3, "Software Power-Down Mode"	• Under the second bullet entitled “Voltage Regulator Controller (LDO)” the sub-bullet text has changed from: “The LDO controller can be disabled by setting the active low LDO enable bit in the Analog Control Register 11. An external source of 1.2V is necessary for operation in this case." to: “The LDO has been defeatured and **LDO_O** should be left disconnected. Microchip recommends disabling the LDO output by setting the active low LDO enable bit in the Analog Control Register 11. An external source of 1.21V is required for operation.”
	Section 6.6.2, "Power Sequence Timing"	• First two paragraphs in this section have been modified. Text changed from: “The recommended power-up sequence is to have the transceiver (VDDAH, VDDAH_x) and digital I/O (VDDIO, VDDIO_1) voltages power up before the 1.1V core (VDDCORE, VDDAL_x, VDDTXL_SERDES) voltage. If the 1.1V core must power up first, the maximum lead time for the 1.1V core voltage with respect to the transceiver and digital I/O voltages must be 200 µs. There is no power sequence requirement between transceiver (VDDAH, VDDAH_x) and digital I/O (VDDIO, VDDIO_1) power rails.” to: “There is no power sequence requirement between transceiver (VDDAH, VDDAH_x), 1.1V core (VDDCORE, VDDAL_x, VDDTXL_SERDES), and digital I/O (VDDIO, VDDIO_1) power rails.” • The following statement has been removed: “The recommended power-down sequence is to have the 1.1V core voltage power-down before powering down the transceiver and digital I/O voltages.”
	Table 6-14, "Power Sequencing Timing Values"	• “tvr” row updated. Previously, Min column had no value, Max was 200 and the Units were in µs. Update changed Min to 0.1, Max to 100 and Units to ms.
DS00003591G (06-21-24)	Table 3-5, "Miscellaneous Pins"	• In description for General Purpose I/O, inserted a table from Errata document regarding buffer type configuration, replacing a now obsolete note. • Renamed “test_a1_a2_en” to “disable_mdo_drv”

TABLE A-1: REVISION HISTORY (CONTINUED)

Revision	Section/Figure/Entry	Correction
DS00003591F (04-13-23)	Product Identification System	• Added Silicon Revision
	Table 5-12, "JTAG Op Codes"	• Op Codes “EXTEST_PULSE” and “EXTEST_TRAIN” removed from table and marked as “RESERVED”.
	Section 6.0, "Operational Characteristics"	• Absolute Maximum Ratings Supply Voltage (**VDDAL_x, VDDTXL_SERDES, VDDCORE**) changed from “-0.5V to +1.21V” to “-0.5V to +1.27V”.
	Section 6.2, "Operating Conditions**"	• Operating Conditions Supply Voltage (**VDDAL_x, VDDTXL_SERDES, VDDCORE**) changed from “+1.16V to +1.21V” to “(-5%/+5%) +1.15V to +1.27V”.
	Table 6-4, "Worst-Case Four Port (1.27V, 3.465V, 3.465V) Power Consumption", Table 6-5, "Worst-Case Four Port (1.27V, 2.625V, 2.625V) Power Consumption", Table 6-6, "Worst-Case Four Port (1.27V, 2.625V, 1.89V) Power Consumption"	• All Worst-Case power numbers updated.
DS00003591E (10-05-22)	Table 1-1, "General Terms", Section 5.11.2, Non OPEN Alliance Low Pass Filtered Error	• Corrected errant SQI definitions
	Figure 4-2 QSGMII MAC Interface Connections	• Corrected **QSGMII_TXP/TXN** and **QSGMII_RXN/RXP** connections to MAC.
	Section 5.11.2, Section 5.11.3, Section 5.11.4, Section 5.11.5	• Corrected note to reference Extended Page 1.
	Section 5.11.4	• Corrected reference to “sqi_squ_mode_en” in second note
DS00003591D (07-06-22)	All	• Added notice of antiquated terminology statement to second page • Removed LDO references throughout document
	Table 3-1, "Pin Assignments"	• Updated **GPIO9/TMS** and **GPIO10/TCK** reset states to “Z”.
	Table 3-5, "Miscellaneous Pins"	• Updated MDIO description with additional details about high-speed MDIO operation.
	Section 5.7, LinkMD Cable Diagnostics	• Expanded section to include 3 new subsections.

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TABLE A-1: REVISION HISTORY (CONTINUED)

Revision	Section/Figure/Entry	Correction
	Table 5-4, "1000M SQI Performance" & Table 5-5, "100M SQI Performance"	• Replaced SQI Value Correlation table with two new tables (1000M and 100M speeds).
	Section 5.14, MIIM (MDIO) Interface	• Added note to end of section: “This device may respond to Clause 45 accesses and so must not be mixed with Clause 45 devices on the same MDIO bus.”
	Section 5.14.1, High-Speed MDIO Operation	• Added new section.
	Section 6.1, Absolute Maximum Ratings*	• Added HBM ESD rating.
	Section 6.2, Operating Conditions**	• Updated **VDDAL_*x*, VDDTXL_SERDES, VDDCORE** supply voltage operating range. • Updated **VDDAH, VDDAH_*x*, VDD33REF, VDDIO, VDDIO_1** supply voltage maximum operating voltage to +5%.
	Section 6.3, Power Consumption	• Updated power consumption numbers.
	Table 6-14, "LDO Controller" (Table removed in Rev. H)	• Updated “Output of P-channel MOSFET” to 1.1V min, 1.16V typical, 1.21V max.
	Section 6.6.2, Power Sequence Timing	• Updated Figure 6-2. • In Table 6-14, replaced t_{svsc} row with new t_{scrd} row.
	Table 6-15, "RESET_N Configuration Strap Timing"	• Replaced t_{css}, t_{csh}, and t_{odad} “TBD” with 5 ns, 5 ns, and 3.5 us, respectively.
	Section 6.6.5, MDC/MDIO Timing	• Added additional sentence regarding high-speed MDIO operation.
	Table 6-21, "Crystal Specifications"	• Replaced Crystal Startup Time “TBD” with “<2 ms”.
DS00003591C (02-01-22)	General	Removed confidential marking.
DS00003591B (11-17-21)	General	Changed temperature range for commercial parts to “0°C to 85°C” and for industrial parts to “-40°C to 85°C”.
	Cover	Updated Time Sensitive Networking bullet for clarity: “Time Sensitive Networking (TSN) Frame Preemption support per IEEE 802.3-2018 clause 99”.
	Table 1-1	Added 10BASE-Te definition.
	Table 1-2, Table 3-3, Table 3-4, Table 6-8	• Updated LVDS buffer type to LVDS1 and LVDS2 • CLK125_REF_INP/INM assigned LVDS1, REF_PAD_CLK_P/M assigned LVDS2 • Updated buffer characteristics to include both LVDS1 and LVDS2

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TABLE A-1: REVISION HISTORY (CONTINUED)

Revision	Section/Figure/Entry	Correction
	Figure 3-1, Table 3-1	Updated the following port 2 and port 3 VDDAL ADC naming conventions to match silicon revision B0: • **VDDAL_ADC_D_P2/P3** changed to **VDDAL_ADC_A_P2/P3** • **VDDAL_ADC_C_P2/P3** changed to **VDDAL_ADC_B_P2/P3** • **VDDAL_ADC_B_P2/P3** changed to **VDDAL_ADC_C_P2/P3** • **VDDAL_ADC_A_P2/P3** changed to **VDDAL_ADC_D_P2/P3**
	Figure 3-1	Updated Pin 1 orientation
	Table 3-1	Changed **MDIO** and **MDC** pin reset states to Z
	Table 3-4	Updated **CK25OUT** definition to include: “This output clock is powered by **VDDAH**.”
	Table 3-5	• Added additional information to **MDIO** description • Removed pull-ups on **MDIO** and **MDC** pins • Updated **REF_CLK_SEL[1:0]** definition for 01 to “RESERVED” and added note
	Table 3-7	• Added note to **PHYAD[4:0]** definition: “**PHYAD[4:0]** must not be greater than ‘h1C.”
	Table 3-9	• Updated “01001” definition to RESERVED • Added legend entry to indicate what ‘X’ means • Changed ‘y’ to ‘X’
	Section 4.1, Voltage Regulator and Power Connections	Corrected electrolytic capacitor value to 220 µF
	Figure 4-1	• Updated to separate **VDDAL_SERDES** and **VDDTXL_SERDES** into two separate ferrite beads • Added RC circuit to **VDDAH_PLL_PTP** signal
	Figure 4-2	Updated to include note on external termination resistor.
	Figure 4-3	• Corrected RJ-45 pins (+/-) • Added note under figure “The device supports integrated connector magnetics with ganged center taps.”
	Section 4.1.1, MOSFET Selection	Added sentence to end of section: “A 300 µF electrolytic capacitor between 1.1V and ground is required for proper LDO operation.”
	Table 5-6	Changed 5-bit MII Read and Write PHY register addresses from “00AAA” to “AAAAA”
	Table 5-10	Updated Enhanced Mode 12 descriptions

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TABLE A-1: REVISION HISTORY (CONTINUED)

Revision	Section/Figure/Entry	Correction
	Section 5.9, IEEE 802.3-2018 Frame Preemption, Section 5.10, Start of Frame Indication	Updated “802.3br-2016” references to “802.3-2018/PTP”
	Section 5.16, GPIOs	Corrected number of GPIOs from 23 to 24
	Section 5.20.3, Resets	Updated descriptions to detail Gigabit PHY reset. Clarified/added sub-bullets. Removed mention of Analog Common VCO reset. Removed “Gigabit PHY PCS (per port)” bullet
	Section 6.1, Absolute Maximum Ratings*	Corrected **VDDAL_*x***, **VDDTXL_SERDES**, **VDDCORE** supply voltage max to 1.21V
	Section 6.3, Power Consumption	• Added power consumption data • Updated description to indicate worst-case measurements taken at 125°C junction temperature
	Table 6-14 (Table removed in Rev. H)	Added notes under table
	Table 6-20	Updated table values, removed TBDs
	Product Identification System	• Removed “TBD” and changed it to “ZMX” • Removed Tape & Reel information
DS00003591A (08-19-20)	All	Initial release

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PRODUCT IDENTIFICATION SYSTEM

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PART NO.	[-X]	/	XXX	RR
Device	Temp.		Package	Silicon Revision

Device:	LAN8804	
Temperature:	Blank	= 0°C to +85°C (Commercial)
	V	= -40°C to +85°C (Industrial)
Package:	ZMX	= 128-pin TQFP (9.0 mm ePad)
Silicon Revision:	Blank	= Silicon Revision prior to C1
	C1	= Silicon Revision C1

Examples:

a) LAN8804/ZMXC1
128-pin TQFP, Tray,
Commercial Temperature, Silicon Revision 1

b) LAN8804-V/ZMXC1
128-pin TQFP, Tray,
Industrial Temperature, Silicon Revision 1

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