Ensuring high performance of AI chip designs

Artificial intelligence (AI) systems and their large data sets, machine learning algorithms, and computing hardware present significant opportunities and equally huge hurdles.

AI accelerators (chips) enable the processing of vast amounts of data and perform complex computations at lightning speed. To do so they consume more power than the highest-wattage processors before them. These power levels create a larger amount of heat across datacenters and hyperscale datacenters. A mounting concern is achieving needed cooling to efficiently eliminate excess heat.



Cooling: A designer's dilemma

At current AI chip wattages, many thermal interface materials do not possess the low thermal resistance needed to efficiently transfer these large heat loads. The results can be temperature spikes, slower and sometimes failing processors. Maximizing conductive heat transfer is the goal. The challenge is heightened as device power densities increase, along with the increasing need to reduce energy costs associated with cooling.

Offered by Avnet, Laird Technologies' thermal interface materials portfolio is growing steadily. Laird™ Tpcm™ 7000, Tgrease™, and Tgel™ thermal gel products each offer industry-leading lowest

thermal resistances addressing the challenges of the AI market. We drive for next generation performance while working to solve customers' concerns about long-term reliability, many times collaborating on application-specific testing systems. We go all the way to ensure we are providing the best solution.



Laird Tpcm 7000 phase change material

[See the short application video]

EMI: A second serious AI design threat

As higher-powered AI chip designs emerge, a second and sometimes interrelated concern alongside heat is excessive electromagnetic interference. EMI has always plagued chips with high power densities. Now, increasingly powerful AI chips and extreme board densities worsen EMI concerns even more.

In applications such as data centers, long-term AI chip performance faces formidable obstacles. Several types of unwanted noise emanate from chips, ranging from the chip architecture itself through device verification. The threat EMI poses to AI chips casts a shadow across the PCB.



Address noise early

Designers creating AI chip architecture should plan to address and resolve EMI early in their development cycle. They should consider tradeoffs in early design phases. Among them are noise (such as device crosstalk), wattage, low and high frequency applications, linearity, and board density.

Laird solutions are the choice worldwide to stem troublesome EMI, including our short wavelength absorbers delivering reliability to meet AI's higher frequency trends such as faster, larger bandwidth data flow. AI device designers often need wide-ranging options. One way we help is an extremely broad absorber line of solid sheet, dispensable, and 3D thermoplastic designs.

Customers also benefit from Laird's world-class modeling, simulation, and predictive analytics capabilities which deliver answers leading to faster compliance and commercialization.

One emerging trend is the growing number of board design teams opting for multichannel "all-in-one" solutions with the capability of addressing thermal and EMI challenges along with shrinking board space in a single, highly compact, and space-saving package.